

Errata

Title & Document Type: 59313A Analog to Digital Converter Operating and Service Manual

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OPERATING AND SERVICE MANUAL

ANALOG TO DIGITAL CONVERTER

59313A



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**MODEL
59313A
ANALOG
TO DIGITAL
CONVERTER**

SERIALS PREFIXED: 1608A

This manual applies directly to instruments with serial numbers prefixed with 1608A. For other serial prefix numbers, refer to the publication change notices or manual change pages supplied.

**OPERATING AND SERVICE MANUAL
59313-91999**

**MICROFICHE NUMBER
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SECTION I GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This manual describes the Hewlett-Packard Model 59313A Analog to Digital Converter, its specifications (Table 1-1), its installation in a Hewlett-Packard Interface Bus (HP-IB) system, its programming code requirements and output, how it operates, and how to trace malfunctions to a particular circuit board. Complete parts identification information and schematic diagrams are provided at the rear of this manual, together with lists of options and accessories supplied. Available accessories are listed in Table 1-2.

1-3. DESCRIPTION.

1-4. The Model 59313A Analog to Digital Converter changes analog signals in four ranges to 11-bit two's complement binary data, in two eight-bit bytes (see Specifications, Table 1-1). It is programmed by a system controller, such as an HP Model 9825A Calculator, through the HP Interface Bus System, over which it sends the converted data to the controller. The Converter can be programmed to make a single conversion, or run at selected pace rates of up to 200 per second on one channel or up to 50 per second on each of four channels. When control of sampling from outside the Converter is enabled, it may be initiated by an external TTL logic transition or contact closure to ground, in synchronization with the external process being measured. The Converter has a program-controlled reverse channel capable of driving small lamps, relays, or TTL devices. Each channel is connected to a calibration voltage when its plug is removed from the corresponding rear panel input jack.

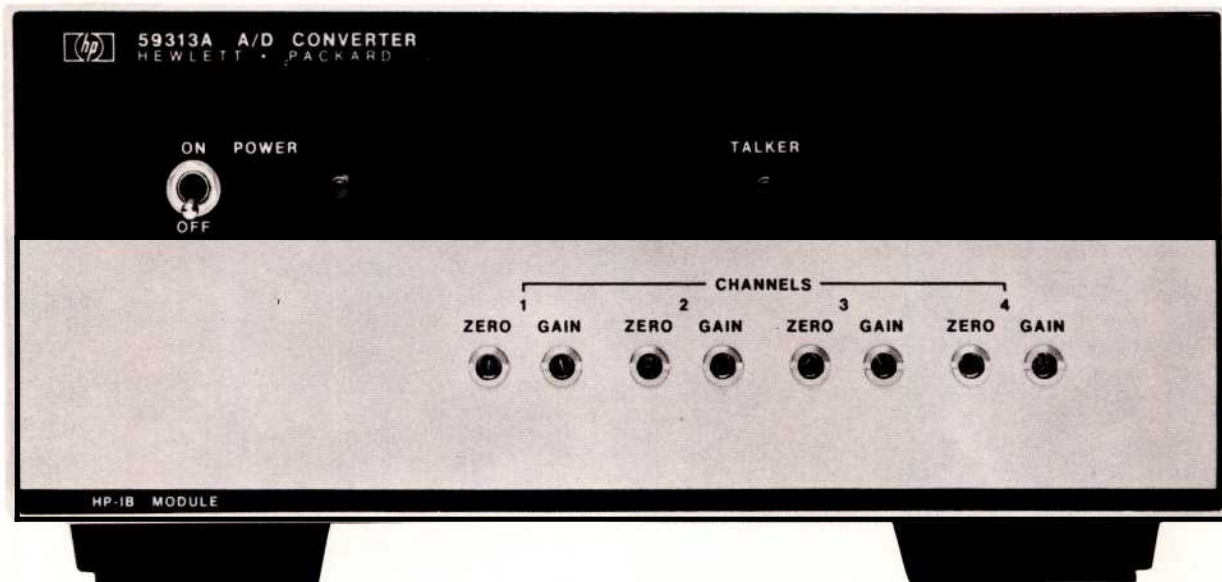


Figure 1-1. Model 59313A A/D Converter

Table 1-1. Specifications

ANALOG INPUTS

No. and Type: 4 each, single ended, bipolar.
Full Scale Voltage Ranges (Jumper Selectable):
 ±1.0 to ±1.3V ±5.0 to ±7.0V
 ±2.5 to ±3.5V ±7.0 to ±10.3V

Gain Trim (Front Panel): Screwdriver adjustment provides fine gain trim within ranges.

Zero Trim (Front Panel): Screwdriver adjustment provides ±2% of full scale trim.

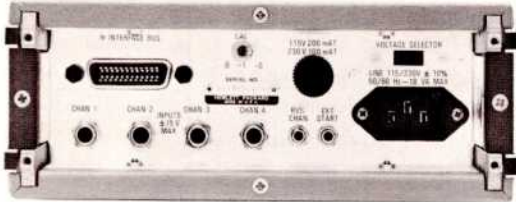
Input Impedance: Greater than 1 megohm.

Maximum Input Voltage: 30V rms without damage.

Crosstalk: Less than 1/2 LSB on any channel with all other channels connected to the same full scale 100 Hz sine wave.

Input Connectors (Rear Panel): Standard phone jack; tip-hi, ring — signal GND, sleeve — chassis GND.

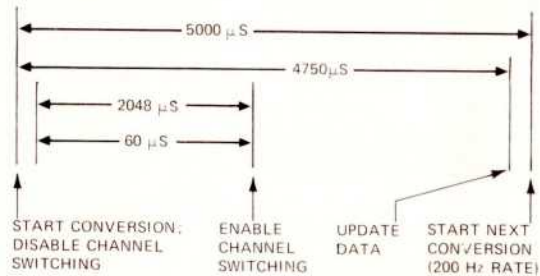
Calibration Reference: 0V, -1.0V, -5.0V, ±0.1%; selectable by switch on rear panel. Appears on those channels with no input plug inserted.



Program Commands: The 59313A responds to the following program characters:

- | | |
|---------------------------------|--------------------------|
| A — One conversion only | 1 — Chan 1 |
| B — 200 Hz | 2 — Chan 2 |
| C — 100 Hz | 4 — Chan 3 |
| D — 50 Hz | 8 — Chan 4 |
| E — 20 Hz | |
| F — 10 Hz | |
| G — 5 Hz | Universal Bus Commands |
| H — Reset (all except rev. ch.) | |
| I — Stop (pacer) | Binary |
| J — Start (pacer) | Equiv. |
| K — External Start Enable | 20 — Device Clear |
| L — SRQ Enable | 24 — Serial Poll Enable |
| M — SRQ Disable | 25 — Serial Poll Disable |
| N — Reverse Chan. ON | 63 — Unlisten |
| O — Reverse Chan. OFF | 95 — Untalk |

Converter Timing: (For complete details see Operating Manual.)



A-TO-D CONVERTER

Type: Dual Slope.

Resolution: .05%, 10 bits plus sign.

Nonlinearity: Less than 1/2 LSB.

Conversion Time: 4.75 ms.

Converter Timing: (See timing diagram at right.)

Output Code: 11-bit, two's complement binary output in two 8-bit bytes:

1st Byte							
B11	B11	B11	B11	B11	B11	B10	B9
2nd Byte							
B8	B7	B6	B5	B4	B3	B2	B1

B11 = MSB (sign); B1 = LSB

PACER

Sample Rates: 5, 10, 20, 50, 100, 200 per second.

Accuracy: ±.05%.

External Start (Rear Panel): When enabled, TTL transition or contact closure to ground on miniphone jack will start the pacer synchronously.

REVERSE CHANNEL

Type: Open collector transistor.

Connector (Rear Panel): Miniphone jack.

Open Circuit-Voltage: +60V maximum.

Sink Current: 200 mA maximum.

BUS INTERFACE

Address Selection: Internal jumpers. Factory set to:

LISTEN = &
 TALK = F

Service Request: When enabled, SRQ line goes Lo when data is ready.

Talker Lamp (Front Panel): Lights when 59313A is the bus talker and attention is not active.

Bus Connector (Rear Panel): 24-pin connector; mates with cable HP 10631A/B/C/D.

ENVIRONMENTAL

Operating Temperature: 0°C to +55°C

Storage Temperature: -40°C to +70°C.

Relative Humidity: To 95% at 40°C.

STABILITY

Gain Change: Less than ±0.6% of reading from 0° to 55°C
Zero Change: Less than ±0.3% of full scale.

POWER REQUIREMENTS

Voltage (Rear Panel Selectable): 115V ac or 230V ac ±10%, 48—66 HZ.

Power Consumption: 18 VA maximum.

MECHANICAL

Height: 8.9 cm (3.5 in.) without feet, 10.2 cm (4 in.) with feet.

Width: 21.2 cm (8.4 in.).

Length: 35 cm (13.8 in.).

Net Weight: 3.6 kg (8 lb.).

ORDERING INFORMATION

Accessories Supplied: 2.4 m (8 ft.) power cord, operating and service manual, adjusting screwdriver, operating card.

OPTIONS

Option 001: Medical white front panel.

Option 003: 76 cm (30 in.) power cord, CEE to CEE.

Option 030: 76 cm (30 in.) NEMA power cord.

Option 038: 2.4 m (8 ft.) power cord, CEE to CEE.

Option 090: 2.3 m (7.5 ft.) U.K. power cord.

Option 092: 2 m (6.6 ft.) W. Eur. power cord.

ACCESSORIES AVAILABLE

14221A: Miniphone to miniphone cable, 3.0 m (10 ft.).

14331A: Phone to GND cable, 1.8m (6 ft.).

10631A: Bus cable, 0.9 m (3 ft.).

10631B: Bus cable, 1.8 m (6 ft.).

10631C: Bus cable, 3.6 m (12 ft.).

10631D: Bus cable, 0.5 m (1 1/2 ft.).

SECTION II INSTALLATION

2-1. INTRODUCTION.

2-2. This section contains information on installing the Hewlett-Packard Model 59313A A/D Converter into Hewlett-Packard Interface Bus Systems.

2-3. INITIAL INSPECTION.

2-4. Mechanical Inspection.

2-5. If external damage to the shipping carton is evident, ask the carrier's agent to be present when the unit is unpacked. Check the instrument for external damage, such as broken controls or connectors, and dents or scratches on the panel surface. If damage is found, refer to Paragraph 2-8 for recommended claim procedure and repacking information. If the shipping carton is not damaged, check the cushioning material and note any signs of severe stress as an indication of rough handling in transit. Retain the packaging material for possible future use.

2-6. Electrical Check.

2-7. Check the electrical performance of the unit as soon as possible after receipt; see Paragraph 5-7 for the recommended performance checks. The checks will verify that the instrument is operating within the specifications listed in Table 1-1. This check is a good test procedure for incoming quality control inspection and for an operational check after repairs or adjustments have been made.

2-8. CLAIMS AND REPACKAGING.

2-9. Claims for Damage.

2-10. If physical damage is evident or if the instrument does not meet specifications when received, notify the carrier and the nearest Hewlett-Packard Sales/Service Office. The Sales/Service Office will arrange for repair or replacement of the unit without waiting for settlement of the claim against the carrier.

2-11. Packaging for Reshipment or Storage.

2-12. If the instrument is to be shipped to a Hewlett-Packard Sales/Service Office, attach a tag showing name and address of owner, instrument model and serial numbers, and the repair required or a description of the trouble. The original shipping carton and packaging material may be reusable. The Hewlett-Packard Sales/Service Office will also provide information and recommendations on materials to be used if the original packaging material is not available or not reusable.

2-13. PREPARATION FOR USE.

2-14. Environment.

2-15. System location should be reasonably free from vibration, dust, corrosive or explosive vapors or gases, and extremes of temperature or humidity. For a cabinet mounted installation, allow sufficient room at the front for operation and sufficient room at the rear for servicing with the cabinet access door open.

Section II — Installation
Model 59313A

2-16. The Model 59313A operates within specifications at ambient temperatures between 0°C and 55°C. Ambient temperatures exceeding these limits could affect the accuracy of the instrument and cause damage of the components and circuits. Allow at least two inches clearance around the instrument for air circulation.

2-17. Fuse.

2-18. The fuse, Figure 2-1(3), is selected for the ac line voltage in use. To replace a blown fuse,

- a. Push in on the cap, turn counterclockwise 1/4 turn, and pull out.
- b. Pull the fuse out of the cap, and replace it with a fuse of the correct rating, (rating is stamped on one of the fuse ends), 2/10A for 115V, 1/10A for 230V.

CAUTION

FAILURE TO USE THE CORRECT FUSE CAN RESULT IN LOSS OF THE PROTECTION IT IS DESIGNED TO GIVE, OR MAY CAUSE THE FUSE TO KEEP BLOWING.

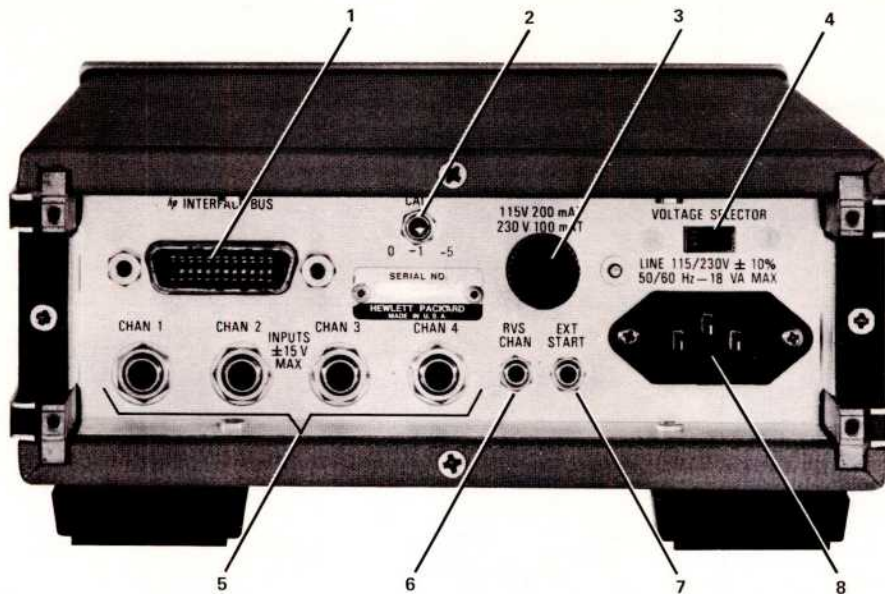
2-19. Coarse Range Selection.

2-20. Each of the four analog channels has four possible input ranges:

- LO = full scale between ± 1.0 and ± 1.3 volts
- MED = full scale between ± 2.5 and ± 3.5 volts
- HI = full scale between ± 3.5 and ± 5.0 volts
- HI-HI = full scale between ± 7.0 and ± 10.3 volts

These ranges are selected by a jumper wire placed between pins on the bottom board inside the 59313A.

- a. For access to these jumpers:
 - (1) Disconnect the ac power cord.
 - (2) Remove the top cover (1 screw, center rear).
 - (3) Remove the 4 outermost screws from the circuit board.
 - (4) Just in front of the black transformer, slip the forefinger under the top and middle circuit boards and pull up to disengage the connector.
 - (5) Remove the top and middle circuit boards together, exposing the bottom board range jumpers.
- b. Select the best input range:
 - (1) Determine the full scale analog voltage output of the device to be connected to that channel.
 - (2) Use the lowest range possible, but the full scale analog input voltage must not be greater than the high limit listed for that range.
 - (3) Refer to Figure 2-2 and make the proper jumper connections.



1. **HP-IB CONNECTOR:** ACCEPTS STANDARD HP INTERFACE BUS CABLE USED TO CONVEY DATA AND PROGRAMMING INSTRUCTIONS BETWEEN THE 59313A AND THE BUS CONTROLLER.
2. **CAL SWITCH:** SWITCHES 0, -1, or -5 CALIBRATION VOLTAGE TO ANY ANALOG INPUT CHANNEL THAT DOES NOT HAVE A PHONE PLUG INSERTED.
3. **FUSE:** PROVIDES OVER-CURRENT PROTECTION IN EVENT OF INTERNAL FAILURE OR ACCIDENTAL SHORT CIRCUIT.
4. **LINE VOLTAGE SELECTOR SWITCH:** PROVIDES FOR 115 OR 230 VOLT LINE OPERATION, WHEN IT IS PLACED IN POSITION CORRESPONDING TO AVAILABLE LINE VOLTAGE USING SCREWDRIVER OR SIMILAR TOOL.

CAUTION

SWITCH MUST BE IN CORRECT POSITION TO PREVENT INSTRUMENT DAMAGE.

5. **ANALOG INPUT JACKS:** ACCEPT FOUR STANDARD 1/4-INCH DIAMETER PHONE PLUGS WITH THE ANALOG INPUT SIGNAL CONNECTED TO TIP, SIGNAL GROUND TO RING, AND SHIELD TO SLEEVE. FULL SCALE VOLTAGES OF ± 1 TO ± 10 CAN BE ACCOMMODATED ON EACH CHANNEL, INDEPENDENT OF THE OTHER CHANNEL RANGES. COARSE RANGES ARE SELECTED BY JUMPERS INSIDE THE 59313A AND FINE INPUT ADJUSTMENTS ARE MADE WITH THE FRONT PANEL GAIN CONTROLS. ANY INPUT JACK THAT DOES NOT HAVE A PHONE PLUG INSERTED IS AUTOMATICALLY CONNECTED TO THE CALIBRATION VOLTAGE.

CAUTION

TO PREVENT INSTRUMENT DAMAGE, DO NOT APPLY MORE THAN 30 VAC (RMS) TO THE INPUT JACKS.

6. **REVERSE CHANNEL JACK:** CONNECTS THE INSTRUMENT TO BE DRIVEN BY THE REVERSE CHANNEL. THE RVS CHAN JACK ACCEPTS A STANDARD 1/8-INCH DIAMETER MINI PHONE PLUG WITH SIGNAL CONNECTED TO TIP AND GROUND CONNECTED TO SLEEVE. THE CHANNEL IS A PROGRAMMABLE NPN TRANSISTOR SWITCH CLOSURE TO GROUND, REQUIRING AN EXTERNAL SUPPLY. WHEN OFF, IT SINKS NO CURRENT AND CAN HAVE VOLTAGES IN THE RANGE 0 TO +80 APPLIED. WHEN ON, IT IS GROUNDED AND CAN SINK UP TO 200 mA.

CAUTION

TO PREVENT INSTRUMENT DAMAGE, DO NOT APPLY MORE THAN +80 VDC TO THE REVERSE CHANNEL JACK, OR CURRENT GREATER THAN 0.2 AMPERE.

7. **EXTERNAL START JACK:** CONNECTS THE DEVICE THAT WILL START CONVERSION. THE EXT START JACK ACCEPTS A 1/8-INCH DIAMETER MINI PHONE PLUG WITH SIGNAL CONNECTED TO TIP AND GROUND CONNECTED TO SLEEVE. WHEN ENABLED BY PROGRAM INSTRUCTION, A CONTACT CLOSURE TO GROUND, CONTACT OPENING FROM GROUND, OR EITHER TRANSITION OF A STANDARD TTL DEVICE, WILL INITIATE ONE CONVERSION OR THE FIRST OF A SERIES OF CONVERSIONS, DEPENDING ON THE 59313A OPERATING MODE.

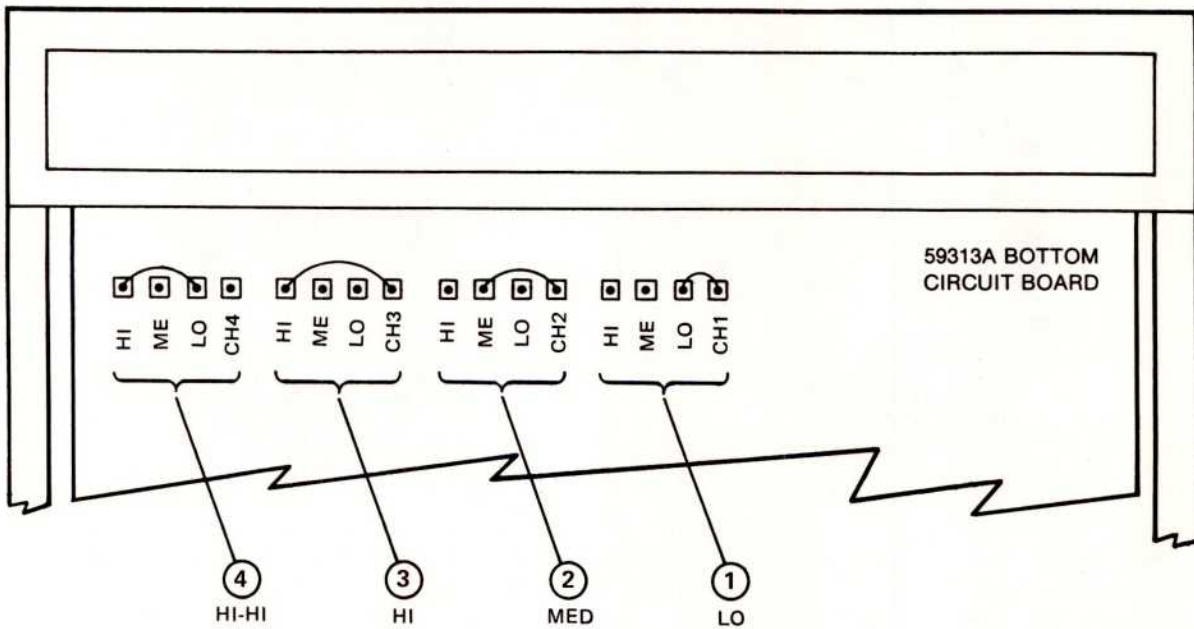
CAUTION

TO PREVENT INSTRUMENT DAMAGE, DO NOT APPLY MORE THAN +5 VDC TO THE EXT START JACK.

8. **AC POWER INLET:** ACCEPTS THE AC POWER CORD USED TO SUPPLY THE INSTRUMENT.

Figure 2-1. Model 59313A Rear Panel

Section II — Installation
 Model 59313A



1. **RANGE SELECTION PINS FOR CHANNEL 1.**
 SHOWN SET TO LOW INPUT RANGE (± 1 TO ± 1.3 VOLTS FULL SCALE).
2. **RANGE SELECTION PINS FOR CHANNEL 2.**
 SHOWN SET TO MEDIUM INPUT RANGE (± 2.5 TO ± 3.5 VOLTS FULL SCALE).
3. **RANGE SELECTION PINS FOR CHANNEL 3.**
 SHOWN SET TO HIGH INPUT RANGE (± 3.5 TO ± 5.0 VOLTS FULL SCALE).
4. **RANGE SELECTION PINS FOR CHANNEL 4.**
 SHOWN SET TO HI-HI INPUT RANGE (± 7.0 TO ± 10.3 VOLTS FULL SCALE). NO JUMPER ALSO GIVES THIS RANGE.
 - A. EACH OF THE FOUR POSSIBLE RANGES HAS BEEN ILLUSTRATED. A SPARE JUMPER IS PROVIDED TO REPLACE ANY THAT MAY BECOME DAMAGED.
 - B. TO CHANGE A JUMPER:
 - (1) HOLD FIRMLY HERE WITH SMALL NOSE PLIERS.
 - (2) TO REMOVE, PULL STRAIGHT UP.
 - (3) TO INSTALL, PUSH STRAIGHT DOWN.

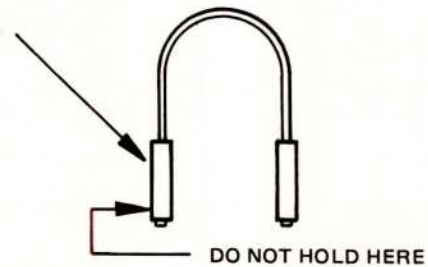


Figure 2-2. Coarse Range Selection

c. Fine adjustment of the range, which must be made after the instrument is reassembled, is discussed in Paragraph 3-48, zero and gain adjustments.

NOTE: Address selection should be made before instrument reassembly, as discussed in Paragraph 2-22.

2-21. ADDRESS SELECTION.

2-22. Each device connected to the Hewlett-Packard Interface Bus (HP-IB) must have its own *unique* address code. Inside the 59313A, the top circuit board has 5 jumpers which permit selection of any of the 31 allowable codes shown in Table 2-1, some of which are shown on the top of the instrument. The instruments are shipped from the factory with the following addresses:

LISTEN address $\boxed{\&}$
TALK address \boxed{F} = device I.D. 06

Unless two or more 59313A's are to be used in one system, or some other device has already been assigned this address, there should be no need to make a change. If a change is necessary, proceed as follows:

- a. Remove the top and middle circuit boards together, as in Paragraph 2-20, part a.
- b. Remove the 2 remaining screws from the top circuit board.
- c. Unplug the middle circuit board from the small connector board to expose the 5 jumpers on the top board.
- d. Consult Table 2-1 for the desired code and Figure 2-3 for the connection method.

NOTE: Never connect the jumpers so that code 11111 is selected as the address. This code is reserved for the UNTALK and UNLISTEN commands.

- e. Reassemble the instrument.
- f. Verify the address selection by sending the TALK address to the 59313A which should turn on the TALKER lamp. Refer to the HP-IB controller manual for instructions on how to send the TALK address.

2-23. Power Cord.

2-24. The power cord is plugged into the ac receptacle on the rear of the instrument (Figure 2-1(8)), and into the local ac supply. Cords with a wide variety of ends are available to mate with the wall outlets in most countries (Figure 2-4). To avoid grounding problems, all the devices used in the system should connect to the same power outlet strip with a common ground. To avoid shock hazard, the integrity of the third wire safety ground must be maintained.

2-25. Interface Bus Cable.

2-26. Bus cables are available as shown in Table 1-2. The cable is connected between the HP-IB connector, Figure 2-1(1), and a similar connector on the controller. The piggy-back cable connector allows connection in a star configuration where all devices connect to the controller connector, or a daisy chain configuration where the first device connects to the controller, and the second device to the first, the

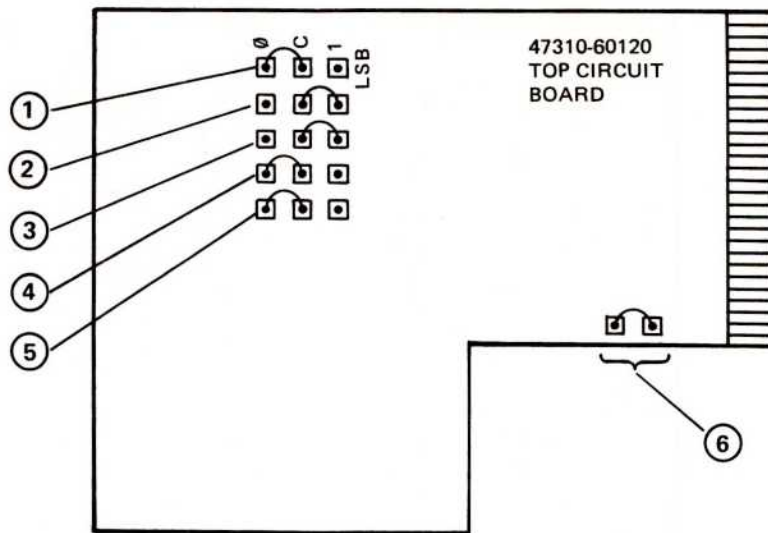
Section II — Installation
Model 59313A

Table 2-1. Allowable Address Codes

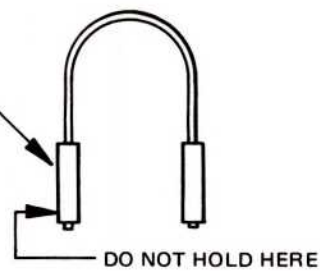
Address Jumpers					Talk Address Character	Listen Address Character	Device I.D. Code
Bit No. 5	Bit No. 4	Bit No. 3	Bit No. 2	LSB Bit No. 1			
0	0	0	0	0	@	SP	0
0	0	0	0	1	A	!	1
0	0	0	1	0	B	"	2
0	0	0	1	1	C	#	3
0	0	1	0	0	D	\$	4
0	0	1	0	1	E	%	5
0	0	1	1	0	F	&	6
0	0	1	1	1	G	' (APOS.)	7
0	1	0	0	0	H	(8
0	1	0	0	1	I)	9
0	1	0	1	0	J	*	10
0	1	0	1	1	K	+	11
0	1	1	0	0	L	, (COMMA)	12
0	1	1	0	1	M	-	13
0	1	1	1	0	N	.	14
0	1	1	1	1	O	/	15
1	0	0	0	0	P	0	16
1	0	0	0	1	Q	1	17
1	0	0	1	0	R	2	18
1	0	0	1	1	S	3	19
1	0	1	0	0	T	4	20
1	0	1	0	1	U	5	21
1	0	1	1	0	V	6	22
1	0	1	1	1	W	7	23
1	1	0	0	0	X	8	24
1	1	0	0	1	Y	9	25
1	1	0	1	0	Z	:	26
1	1	0	1	1	[;	27
1	1	1	0	0	/	<	28
1	1	1	0	1]	=	29
1	1	1	1	0	(>	30
NOTE 2 —	—	—	—	—			

NOTE 1: FACTORY-SET STANDARD ADDRESSES.

NOTE 2: 1 1 1 1 1 IS RESERVED FOR UNLISTEN AND UNTALK. DO NOT SET JUMPERS TO IT.



1. BIT #1 ADDRESS PINS (LEAST SIGNIFICANT BIT)
2. BIT #2 ADDRESS PINS
3. BIT #3 ADDRESS PINS
4. BIT #4 ADDRESS PINS
5. BIT #5 ADDRESS PINS
6. SPARE JUMPER
 - A. TO SET AN ADDRESS BIT TO "ZERO," CONNECT ITS JUMPER WIRE BETWEEN C (COMMON) AND 0 (ZERO).
 - B. TO SET AN ADDRESS BIT TO "ONE," CONNECT ITS JUMPER WIRE BETWEEN C AND 1.
 - C. TO CHANGE A JUMPER:
 - (1) HOLD FIRMLY HERE WITH SMALL NOSE PLIERS.
 - (2) PULL STRAIGHT UP TO REMOVE.
 - (3) PUSH STRAIGHT DOWN TO INSTALL.



NOTE: THE ADDRESS JUMPERS ARE SHOWN FACTORY SET TO 00110 GIVING LISTEN ADDRESS **[&]** AND TALK ADDRESS **[F]**, OR DEVICE I.D. 06.



Figure 2-3. Address Selection Jumpers

Section II — Installation
 Model 59313A

WARNING: REPLACEMENT POWER CABLES MUST PROVIDE CORRECT POLARITY AND GROUNDING AS SHOWN. INCORRECT CONNECTIONS CAN RESULT IN AN ELECTRICAL HAZARD.

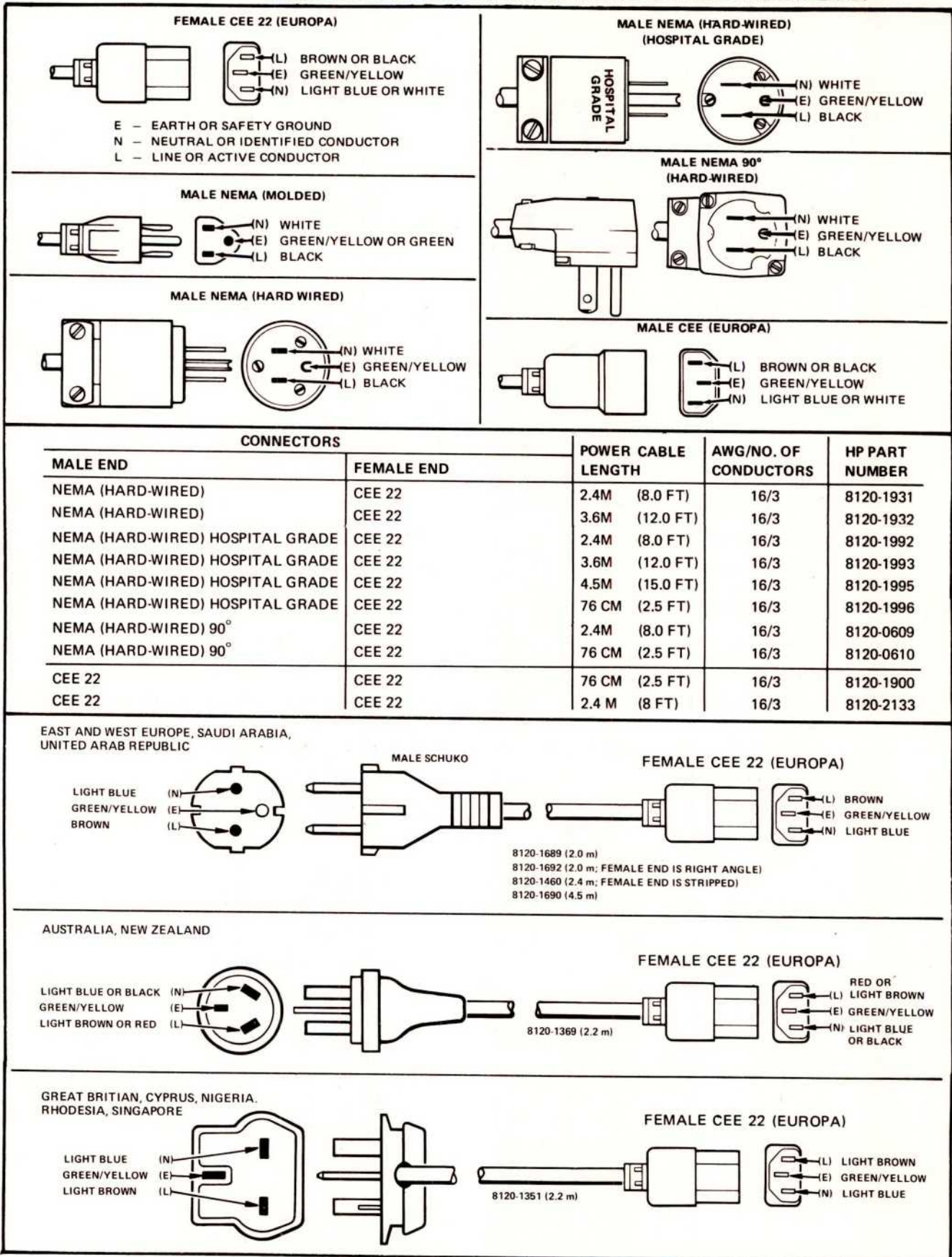


Figure 2-4. AC Power Cables Available

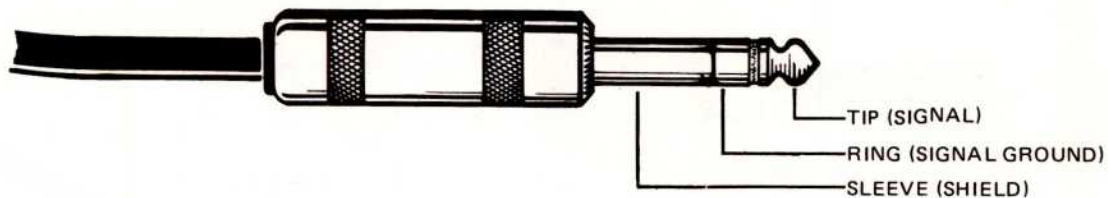


Figure 2-5. Signal Connector Wiring

third device to the second, and so on. A combination of both schemes is also permitted. Six- and twelve-foot standard HP-IB cables can also be used, but the total cable length in the system must not exceed 51 feet. The number of devices in one system must not exceed 15, including the controller. Two types of cable fasteners are in use.

- (1) Chrome-plated U.S. thread 6-32 (up to Spring 1976).
- (2) Black-plated metric thread (after Spring 1976).

All 59313A units have the black metric fasteners. Should one be added to an existing system with chrome U.S. fasteners, all or part of the old system can be updated with metric conversion kits, which consist of new screws for cables and new hex standoffs for instruments.

CAUTION

DO NOT USE DIFFERENT THREAD TYPES TOGETHER.

2-27. Analog Input Cables.

2-28. For each analog input to be used, a shielded cable with a standard 1/4-inch diameter phone plug termination must be provided. The plugs are wired as shown in Figure 2-5.

2-29. Reverse Channel Cable.

2-30. If the reverse channel is to be used, a cable with a 1/8-inch diameter mini phone plug termination must be provided. The plug is wired as shown in Figure 2-6. Note that the reverse channel is a transistor switch to ground and thus requires an external power supply.

2-31. EXTERNAL START CABLE.

2-32. If the external start feature is to be used, provide a cable with a 1/8-inch diameter mini phone plug (Figure 2-6). The cable is connected between the EXT START jack, Figure 2-1(7), and the device that is used to supply the signal. The voltage applied to this jack should not be outside the range 0 to +5 volts.

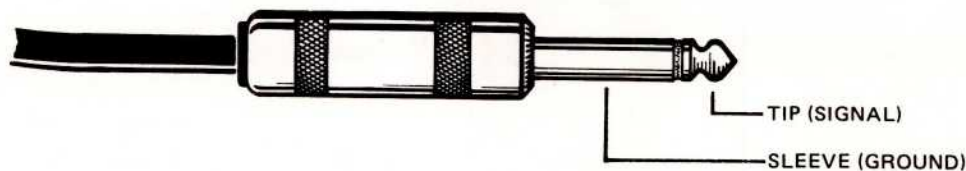


Figure 2-6. External Start and Reverse Channel Connector Wiring

- (1) **HP-IB CONNECTOR:** Accepts standard HP Interface Bus cable used to convey data and programming instructions between the 59313A and the bus controller.
- (2) **CAL SWITCH:** Switches 0, -1, or -5 calibration voltage to any analog input channel that does not have a phone plug inserted.
- (3) **FUSE:** Provides over-current protection in event of internal failure or accidental short circuit.
- (4) **LINE VOLTAGE SELECTOR SWITCH:** Provides for 115 or 230 volt line operation, when it is placed in position corresponding to available line voltage, using a screwdriver or similar tool.

CAUTION

115/230V LINE-VOLTAGE SELECTOR SWITCH MUST BE IN CORRECT POSITION TO PREVENT INSTRUMENT DAMAGE.

- (5) **ANALOG INPUT JACKS:** These jacks accept four standard 1/4-inch diameter phone plugs with the analog input signal connected to TIP, signal ground to RING, and shield to SLEEVE. Full scale voltages of ± 1 to ± 10 can be accommodated on each channel, independent of the other channel ranges. Coarse ranges are selected by jumpers inside the 59313A and fine input adjustments are made with the front panel GAIN controls. Any input jack that does not have a phone plug inserted is automatically connected to the calibration voltage.

CAUTION

TO PREVENT INSTRUMENT DAMAGE, DO NOT APPLY MORE THAN 30 Vac (rms) TO THE INPUT JACKS.

- (6) **REVERSE CHANNEL JACK:** Connects the instrument to be driven by the reverse channel. The RVS CHAN jack accepts a standard 1/8-inch diameter mini phone plug with signal connected to TIP and ground connected to SLEEVE. The channel is a programmable NPN transistor switch closure to ground, requiring an external supply. When OFF, it sinks no current and can have voltages in the range of 0 to +80 applied. When on, it is grounded and can sink up to 200 mA.

CAUTION

TO PREVENT INSTRUMENT DAMAGE, DO NOT APPLY MORE THAN +80 Vdc TO THE REVERSE CHANNEL JACK, OR CURRENT GREATER THAN 0.2 AMPERE.

(7) **EXTERNAL START JACK:** Connects the device that will start conversion. The EXT START jack accepts a 1/8-inch diameter mini phone plug with signal connected to TIP and ground connected to SLEEVE. When enabled by program instruction, a contact closure to ground, contact opening from ground, or either transition of a standard TTL device, the START circuit will initiate one conversion or the first of a series of conversions, depending on the 59313A operating mode.

CAUTION

TO PREVENT INSTRUMENT DAMAGE, DO NOT APPLY MORE THAN +5 Vdc TO THE EXT START JACK.

(8) **AC POWER INLET:** Accepts the ac power cord used to supply the instrument.

NOTES

NOTES

SECTION III OPERATION AND PROGRAMMING

3-1. INTRODUCTION.

3-2. The Model 59313A A/D Converter is controlled by programming from the associated HP Interface Bus Controller. This section provides programming formats and examples that can be used with different controllers to obtain digital data from the 59313A. See Appendix I for a description of the Interface Bus system.

3-3. Operation of the 59313A can be separated into two main divisions:

- (1) Programming the HP-IB Controller to send the 59313A 7-bit ASCII* characters selected from:
 - (a) The CONTROL CHARACTER SET, Table 3-1.
 - (b) The UNIVERSAL BUS COMMAND SET, Table 3-2.

These characters cause the 59313A to perform in the desired manner.

- (2) Programming the HP-IB Controller to extract and use the 59313A output.

3-4. The term "to send" in the following discussion will mean: program the controller to send the required character.

NOTE: Refer to each controller's own manual or its HP-IB interface manual for specific programming instructions.

3-5. Using the Control Character Set.

3-6. Before the 59313A can respond to any control character, it must be made a listener by sending it the listen address code internally selected by jumpers (Figure 2-4). Once the 59313A is addressed, any of the control characters (boxed,) can be sent and the 59313A will respond to them. When the last control character has been sent, the 59313A's *listener state* should be terminated by one of the following:

- (1) Sending the UNLISTEN COMMAND (see Table 3-2).
- (2) Sending the 59313A's TALK ADDRESS (Paragraph 2-22).

3-7. CONTROL TIMING. Each control character's function begins the moment it is received at the 59313A, i.e., not more than 4 microseconds after the controller sets the DAV (data valid) line LO for that character. An exception to this is discussed under switching channels, Paragraph 3-8.

3-8. SWITCHING CHANNELS. A particular channel is selected for conversion when its channel select character is sent. One channel select character should always be in effect if useful conversions are to be made. 100 μ s settling time should be allowed between the time the channel select character is sent and the next conversion is started. Channel switching can be done between conversions but if a channel select character is sent while the converter is in that portion of its cycle where the input signal is needed, then the HP-IB handshake will be inhibited. This means the controller must wait there until the 59313A is finished with the old input before the character selecting the new input will be accepted. This timing is shown graphically in Figure 3-1, and characters are identified in Table 3-3.

NOTE: DO NOT use the character 3 to select Channel 3; use 4 instead, and 8 for Channel 4.

*American Standard Code for Information Interchange, see Appendix IV.

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 Model 59313A

Table 3-1. 59313A Control Character Set

Decimal Code	Octal Code	Binary Code	ASCII Character	Function
49	061	0011 0001	1	Channel 1
50	062	0011 0010	2	Channel 2
52	063	0011 0100	4	Channel 3
56	070	0011 1000	8	Channel 4
65	101	0100 0001	A	One conversion only
66	102	0100 0010	B	5 ms /200 Hz
67	103	0100 0011	C	10 ms /100 Hz
68	104	0100 0100	D	20 ms /50 Hz
69	105	0100 0101	E	50 ms /20 Hz
70	106	0100 0110	F	100 ms /10 Hz
71	107	0100 0111	G	200 ms /5 Hz
72	110	0100 1000	H	Reset
73	111	0100 1001	I	Stop (Pacer)
74	112	0100 1010	J	Start
75	113	0100 1011	K	External Start Enable
76	114	0100 1100	L	Service Request Enable
77	115	0100 1101	M	Service Request Disable
78	116	0100 1110	N	Reverse Channel ON
79	117	0100 1111	O	Reverse Channel OFF

Table 3-2. 59313A Universal Bus Command Set

Decimal Code	Octal Code	Binary Code	ASCII Character	Function
20	024	0001 0100	DC4	Device Clear
24	030	0001 1000	CAN	Serial Poll Enable
25	031	0001 1001	EM	Serial Poll Disable
63	077	0011 1111	?	Unlisten
95	137	0101 1111	—	Untalk

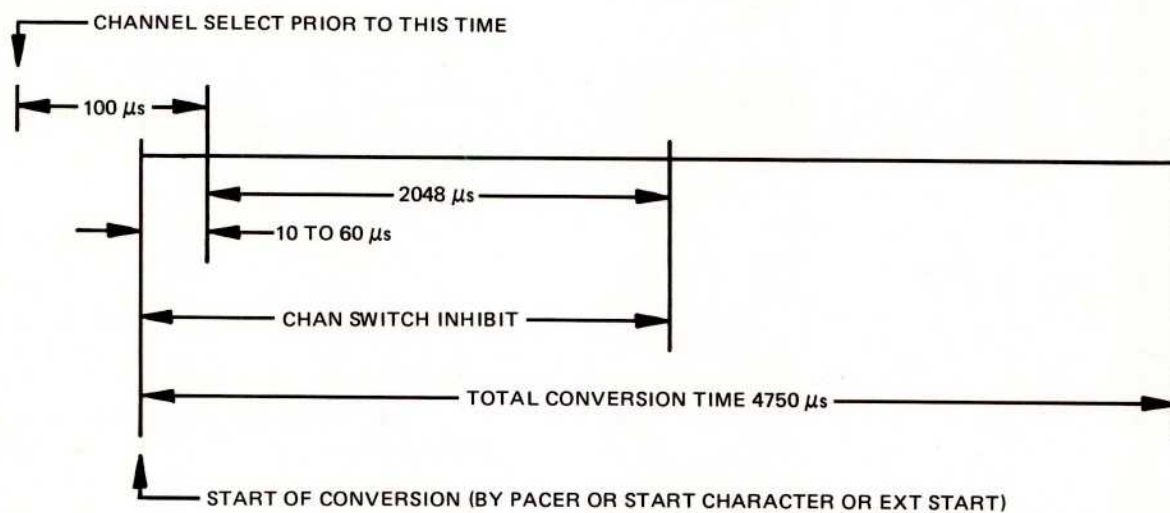


Figure 3-1. Channel Select Timing

Table 3-3. Channel Select Characters

CHANNEL SELECT CHARACTER		
1	CHANNEL 1	Switches on Channel 1 Switches off any other
2	CHANNEL 2	Switches on Channel 2 Switches off any other
4	CHANNEL 3	Switches on Channel 3 Switches off any other
8	CHANNEL 4	Switches on Channel 4 Switches off any other

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3-9. CONTROLLING THE PACE RATE. The pacer is used to start the A to D conversion process.

3-10. The character **A** establishes the single conversion mode. One way to use this mode is by programming the controller with a loop that takes one sample each time thru the loop. This way the spacing between samples is determined by the running time of the controller loop. An example of this type operation is shown in the programming examples, Paragraph 3-39.

3-11. Using one of the characters from Table 3-4 instead of **A** results in the paced mode where the internal pacer starts the conversions at uniform intervals in time. One of the characters **A** thru **G** must be sent or no conversions can be made. Some consideration should be given to the frequency content of the analog input signal when selecting a pace rate. Sampling theory requires a sampling rate greater than twice the highest frequency component present in the input signal to be able to fully reconstruct the signal from the samples. A rate close to 2X would require a fairly sophisticated software routine to reconstruct a sine wave exactly. In practice, a higher sample rate makes reconstruction software much simpler and often unnecessary.

3-12. When the pacer starts, all the pace pulses shown in Figure 3-2 are generated simultaneously, but only the selected one is used to trigger the converter. The first conversion is at $t=0$ and subsequent conversions at the selected interval. If a pace rate is selected without stopping the pacer, the new rate is effective as soon as the character is received by the 59313A. The next conversion will be started by the next pacer output pulse that occurs at the new rate. A pace rate selected when the pacer is not running is stored by the 59313A and used when the pacer is started later. When the pacer is determining the interval between samples, it is important that the controller program used to accept the 59313A output be fast enough to do the job within the selected pace interval.

3-13. Often the running time of the controller program can be checked by taking a large number of samples, say 100 or 1000, and timing the program. At the 10 ms rate, 1001 samples should take $.010 * 1000 = 10$ seconds to run. Since the first sample is at time zero, sample 1001 is at the 10-second point, *not* sample 1000. If it takes more than 10 seconds, the controller is probably not fast enough for the pace interval. Channel switching can be accomplished between conversions started by the pacer if the controller is fast enough to switch the channel and read out the old data within the selected pace interval.

Table 3-4. Pace Intervals

CHARACTER	INTERVAL BETWEEN CONVERSIONS	CONVERSION RATE
B	5 ms	200 PER SECOND
C	10 ms	100 PER SECOND
D	20 ms	50 PER SECOND
E	50 ms	20 PER SECOND
F	100 ms	10 PER SECOND
G	200 ms	5 PER SECOND

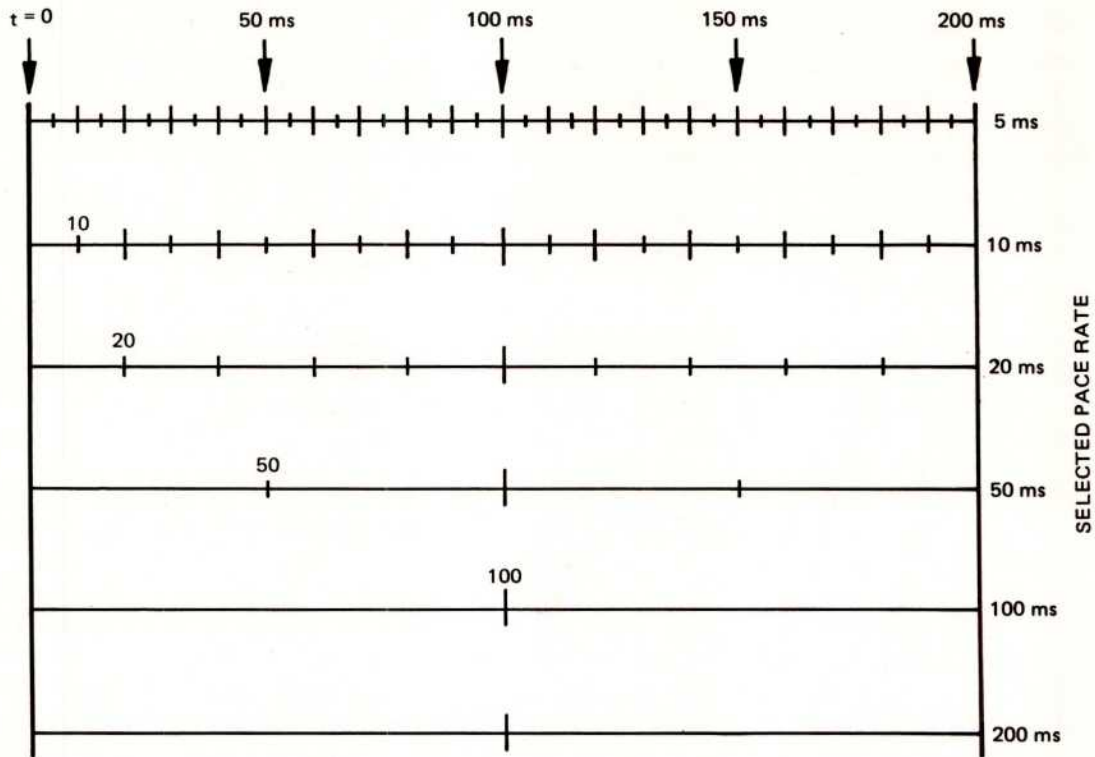


Figure 3-2. Pacer Output Pulses

3-14. STARTING THE PACER (Characters **I**, **J**, **K**). The pacer must be started even if only one conversion is to be made. It can be started in two ways:

- (1) With the control character **J**, START, the pacer starts immediately at the previously selected rate.
- (2) With the control character **K**, EXTERNAL START ENABLE, the pacer waits for a signal at the external start jack before starting at $t=0$ and running at the previously selected rate. The signal can be a contact closure to ground, a contact opening from ground, or either transition of a standard or low power TTL device.

3-15. The pacer will not start unless one of the following has occurred first:

- (1) Sending the **H** = RESET character
- (2) Sending the **I** = STOP character
- (3) Sending the DEVICE CLEAR universal bus command
- (4) Turning on the 59313A power.

The character **I** stops the pacer and arms it for a restart without otherwise affecting the 59313A.

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3-16. CLEARING THE 59313A (Character **H**). The **H** = RESET character is sent to reset the 59313A before it is programmed with a new set of control characters. This character clears the pace selection, clears the channel selection, clears the output register, disables the service request, disables the external start, and arms the start circuit. It does not alter the reverse channel state, or change the 59313A from a listener status. It could add a maximum of about 3 ms to the running time of the controller program if it were sent during a conversion while the converter integrator is at its maximum excursion, thereby taking the maximum reset time.

3-17. SERVICE REQUESTS Characters **L** and **M**). The SRQ (service request) line on the bus can be used to signal the bus controller that the 59313A has data ready for it. This allows the controller to work at another task instead of waiting for data.

3-18. If the SERVICE REQUEST ENABLE character **L** is sent, the SRQ line on the bus will be set LO by the 59313A each time it has completed a conversion and has the output data ready. This occurs about 4.75 ms after the *start-of-conversion* signal. The SRQ line will be cleared (set HI) when the data is transmitted from the 59313A or when a serial poll is conducted.

3-19. If the SERVICE REQUEST DISABLE character **M** is sent, this service request activity ceases without otherwise affecting the 59313A. The 59313A powers up with SRQ disabled, and is also disabled by the RESET character **H**.

3-20. REVERSE CHANNEL (Characters **N** and **O**). The reverse channel is a single digital line that is switched by the controller program, and which may be used to control an external device or process, for instance, to start another process step from which further data can be obtained. If the REVERSE CHANNEL ON character **N** is sent, the open-collector NPN transistor is saturated, thereby sinking currents up to 200 mA to ground. If the REVERSE CHANNEL OFF character, letter **O** is sent, the transistor is turned off and the line appears open-circuited to positive voltages between zero and 80V.

3-21. The two REVERSE CHANNEL characters **N** and **O** can be sent by themselves or included with other control characters. These characters can be repeated a number of times and/or alternated to produce long or short pulses or pulse trains with various duty cycles at the rear panel EXT START connector. Sending the RESET character **H** does not affect the reverse channel.

3-22. The 59313A powers up with the reverse channel OFF. The DEVICE CLEAR COMMAND turns OFF the reverse channel. An external power supply must be used with the reverse channel since it is only a transistor switch to ground. Refer to Figures 3-3 to 3-5 for examples of reverse channel application.

3-23. Using the Universal Bus Command Set.

3-24. When sending these characters the 59313A does not need to be addressed as a listener.

3-25. DEVICE CLEAR (Character **DC4**). When this character is sent to the 59313A, it provides all the reset functions that **H** = RESET does and, in addition:

- (1) The reverse channel is turned off.
- (2) The LISTEN state is ended.
- (3) The TALK state is ended.

It places the 59313A in the same state that it powers up in.

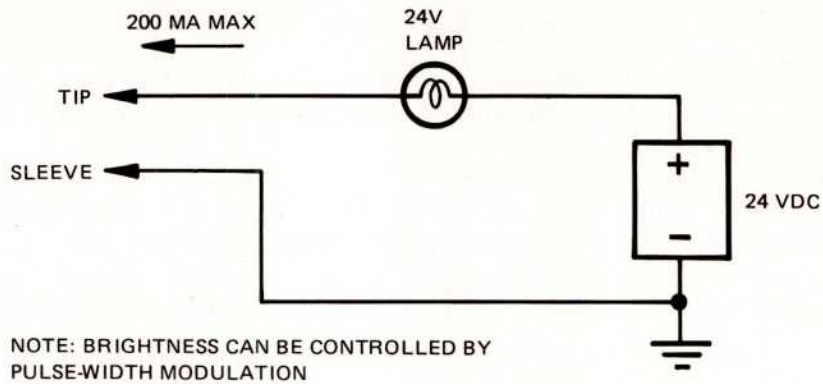


Figure 3-3. Driving a Lamp with the Reverse Channel

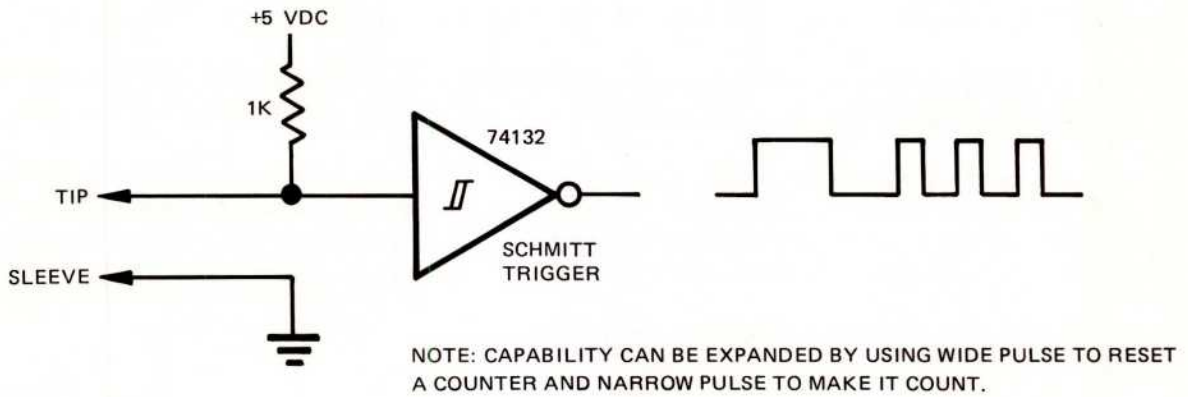


Figure 3-4. Driving TTL Logic with the Reverse Channel

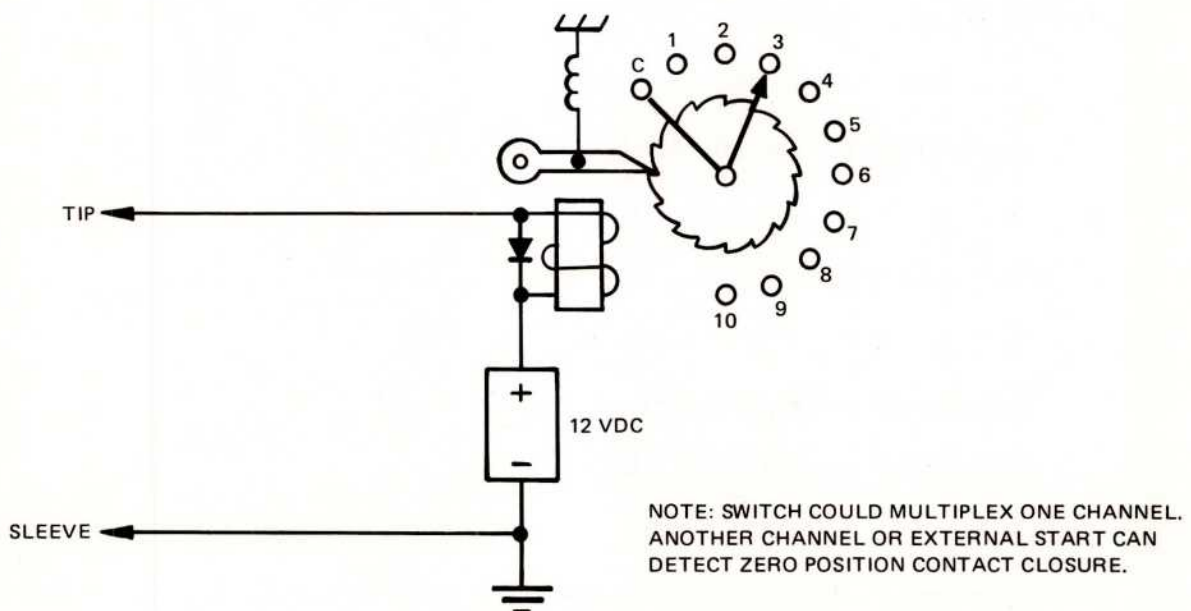


Figure 3-5. Driving a Stepping Switch with the Reverse Channel

Section III — Operation and Programming
Model 59313A

3-26. UNLISTEN (Character ?). This character ends the 59313A LISTEN state, and should be used routinely to insure all unwanted listeners are cleared from the bus before addressing new ones. The 59313A is automatically “unlistened” when it is sent its talk address.

3-27. UNTALK (Character □, underline). This character ends the 59313A TALK state, but is seldom used, because when a new talker is addressed the old one is terminated automatically. The 59313A is also automatically “untalked” when it is sent its listen address.

3-28. SERIAL POLL ENABLE (Character CAN). This character establishes the serial poll mode in the 59313A; the details are described in the output description, Paragraphs 3-35 and 3-36.

3-29. SERIAL POLL DISABLE (Character EM). This character ends the serial poll mode.

3-30. How To Obtain Digital Output Numbers.

3-31. The 59313A becomes the bus TALKER when the controller sends the talk address code set by the internal address jumpers shown in Figure 2-4. When this has been accomplished, the TALKER lamp turns ON and the 59313A can send any data it may have ready to the designated bus listeners, normally the controller.

3-32. NORMAL OUTPUT RESPONSE. If the Serial Poll Enable command has *not* been sent, the output will be the digital conversion of whichever analog input channel was selected by the control character programming.

3-33. The output is an eleven-bit two's complement binary number (see also Appendix II) arranged in two 8-bit bytes as shown in Table 3-5. The output is normally transferred to the controller, which then must reorganize the two bytes into one 11-bit number. The following short program is a generalized (but not necessarily always the most efficient) routine for combining the two bytes that will work for most calculators used as the controller:

- (1) Read 1st byte from 59313A; store it in “A”.
- (2) Read 2nd byte from 59313A; store it in “B”.
- (3) If A is greater than +3, then the number is negative.
- (4) For negative number ($A > 3$):
 - (a) Subtract A from 255 and call it C.
 - (b) Multiply C by 256 and call it D.
 - (c) Subtract B from 256 and call it E.
 - (d) Add D to E and call it F.
 - (e) Multiply F by -1 and use the result.
- (5) For a zero or positive number ($A < 3$):
 - (a) Multiply A by 256 and call it C.
 - (b) Add C to B and use the result.

The programming examples in Paragraph 3-37 show recombining routines for several Hewlett-Packard desktop calculators.

Table 3-5. Output Data Format

BUS LINE →	D108	D107	D106	D105	D104	D103	D102	D101	
1ST BYTE →	B11	B11	B11	B11	B11	B11	B10	B9	
2ND BYTE →	B8	B7	B6	B5	B4	B3	B2	B1	

B11 = MOST SIGNIFICANT BIT = SIGN BIT = 1 IF NEG NUMBER.

B1 = LEAST SIGNIFICANT BIT.

(SEE APPENDIX II ALSO)

3-34. OUTPUT SEQUENCING AND TIMING. The output section is arranged so the following holds true:

(1) The output for a conversion becomes available 4.75 (–0 +.06) ms after the start of conversion and stays available until 4.75 (–0 +.06) ms after the next start of conversion. Conversion starts when \square is received, the external start jack is used, or the pacer time interval is up and a new conversion is started by the pacer (Figure 3-6).

(2) Once both output bytes have been sent, an attempt to send out another byte will result in the bus handshake not being completed (the 59313A will not set DAV line LO) until more data is ready. This feature can often be used to load the controller memory with samples taken by the 59313A at equal increments of time. The controller simply spends its spare time waiting for the handshake to complete. The controller's data acquisition time must be shorter than the 59313A pacer interval being used.

(3) If, when a new pair of data bytes is ready, neither of the old pair has been sent, then the old are replaced with the new.

(4) If, when a new pair of data bytes is ready, the 1st byte of the old pair has been sent but the 2nd has not, then the new pair will be lost and the 2nd byte stays available until it is sent.

3-35. SERIAL POLL OUTPUT RESPONSE. If the Serial Poll Enable command *has* been sent when the 59313A is made the talker, the output will be a poll response instead of the conversion output just described.

3-36. There are two possible poll responses:

(1) AFFIRMATIVE. If the Service Request Enable character \square has been sent and if the 59313A has completed a conversion and set the SRQ line LO prior to the Serial Poll Enable command, then, when made the TALKER, the decimal number 64 would be the output (01000000).

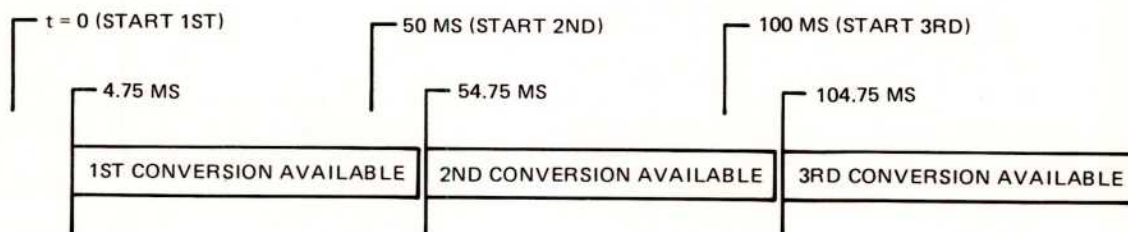


Figure 3-6. 50 Millisecond Pace Rate

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Model 59313A

(2) **NEGATIVE.** If a conversion has *not* been completed and the SRQ line has *not* been set LO by the 59313A (or the SRQ circuitry has not been enabled) prior to the Serial Poll Enable command, then, when made the TALKER, the **decimal number zero would be the output.** Once the Serial Poll Disable command is sent, the 59313A output is again a normal A to D conversion output.

NOTE: The poll response output is just 1 byte of ordinary binary code.

3-37. Programming Examples.

3-38. Send control characters to the 59313A in a logical sequence. For example, do not send the UNLISTEN command immediately after sending the listen address, or do not start the conversion until the desired channel and pace have been selected, or do not send RESET after any of the control characters since it will cancel them all.

3-39. **GENERAL LOOP PROGRAM FORMAT.** The program type with the least chance for error puts the controller into a loop that takes one sample with each repetition. This kind of program is useful for setting the ZERO and GAIN controls discussed later. The general format is:

- (1) Send UNLISTEN command.
- (2) Send 59313A listen address **[&]**.
- (3) It may be necessary to send controller talk address. (See Controller manuals.)
- (4) Send **[H]** RESET character.
- (5) Send **[I]** (or some other) CHANNEL SELECT character.
- (6) Send **[A]** ONE CONVERSION ONLY pace select character.
- (7) Send **[J]** START character (time between **[I]** and **[J]** must be 100 μ s minimum).
- (8) Send 59313A talk address **[F]**.
- (9) It may be necessary to send controller listen address.
- (10) Read and Store 1st byte from the HP-IB.
- (11) Read and Store 2nd byte from the HP-IB.
- (12) Combine 1st and 2nd byte as shown in Paragraph 3-33.
- (13) Display the combined byte as a decimal number.
- (14) Repeat entire loop.

This general program loop will continuously display the 59313A output for Channel 1.

3-40. A translation of the general loop program for the Hewlett-Packard Model 9830A Calculator as the HP-IB controller is:

```

10  CMD "? U &", "H 1 A J", "F 5"
20  DISP ROT (RBYTE 13, 8) + RBYTE 13
30  GO TO 10

```

NOTES:

1. Do not push the SHIFT key if it is not required or the program may not run.
2. Line 20 is a more efficient way of combining the 2 bytes than the general routine shown in the preceding paragraph.

3-41. Two translations are given for the Model 9825A Calculator. The first is the general routine which requires only the GENERAL I/O ROM necessary to use the HP-IB.

NOTE: When using a wrt statement with the 9825A calculator a fmt statement must be used to suppress the carriage returnline feed normally output at the end of the data list.

```

0:  fmt 1, z, f.0
1:  wrt 706.1, "H11AJ"  NOTE: Extra "1" guarantees 100 →s input settling time.
2:  rdb (706) → A
3:  if A>3; gto 5
4:  dsp A*256 + rdb (706)
5:  gto 0
6:  dsp — ( (255—A) * 256 + (256—rdb (706) )
7:  gto 0

```

The second program is a more efficient method that requires both the GENERAL I/O ROM and the EXTENDED I/O ROM.

```

0:  fmt 1, z, f.0
1:  wrt 706.1 "H11AJ"
2:  dsp ior (shf (rdb (706), —8), rdb (706) )
3:  gto 0

```

3-42. A translation for the Model 9820A/21A Calculators is:

```

0:  FXD 0; CMD "?U&", "HaAJ", "5F" |
1:  RDB 13→A; RDB 13→B |
2:  IF A>3; (255—A) * 256 + 256 —B→C; C*—1→C; DISP C |
3:  IF A<3; A*256 +B→C; DISP C |
4:  GTO 00 |

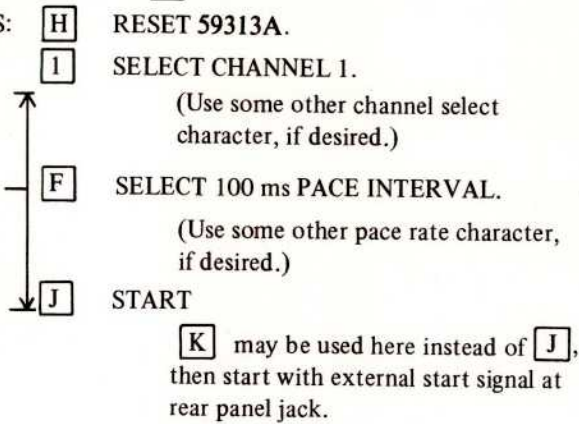
```

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Model 59313A

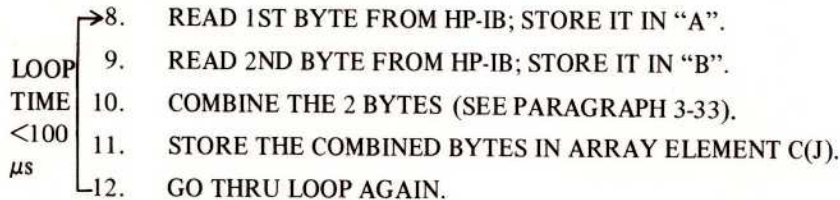
3-43. A program sequence to take samples using the pacer could be:

1. SEND UNLISTEN COMMAND [?].
2. SEND CONTROLLER TALK ADDRESS.
3. SEND 59313A LISTEN ADDRESS [&].
4. SEND CHARACTERS: [H] RESET 59313A.

Time between [I] and [J] should be 100 μ s min. Extra [I] or [F] characters could be sent to add more time if necessary, or use a wait statement, or do some operation that uses up the time.



5. SEND CONTROLLER LISTEN ADDRESS.
6. SEND 59313A TALK ADDRESS [F].
7. SET UP A LOOP WHERE VARIABLE "J" INCREASES BY 1 EACH TIME THRU THE LOOP.



The array "C" will contain samples taken at 100 ms increments in time. Each time thru the loop takes an additional sample. The loop time must be less than the 100 ms pace interval so the controller is always ready when the next 59313A output becomes available.

3-44. A program sequence to take samples using the pacer and also switching channels between samples:

1. SEND UNLISTEN COMMAND [?].
2. SEND CONTROLLER TALK ADDRESS.
3. SEND 59313A LISTEN ADDRESS [&].
4. SEND CHARACTERS: [H] RESET 59313A.
[I] SELECT CHANNEL 1.
[G] SELECT 200 ms PACE INTERVAL.
[J] START.
5. SEND CONTROLLER LISTEN ADDRESS.
6. SEND 59313A TALK ADDRESS [F].
7. SET UP A LOOP WHERE VARIABLE "J" INCREASES BY 1 EACH TIME THRU THE LOOP.

- 8. READ 1ST BYTE FROM HP-IB; STORE IT IN "A".
9. READ 2ND BYTE FROM HP-IB; STORE IT IN "B".
10. COMBINE THE 2 BYTES (SEE PARAGRAPH 3-33).
11. STORE THE COMBINED BYTES IN ARRAY ELEMENT C(J).
12. SEND CONTROLLER TALK ADDRESS.
13. SEND 59313A LISTEN ADDRESS [&] .
14. SEND CHARACTER [2] = SELECT CHANNEL 2.
15. SEND CONTROLLER LISTEN ADDRESS.
16. SEND 59313A TALK ADDRESS [F] .
17. READ 1ST BYTE FROM HP-IB; STORE IT IN "A".
18. READ 2ND BYTE FROM HP-IB; STORE IT IN "B".
19. COMBINE THE 2 BYTES (SEE PARAGRAPH 3-33).
20. STORE THE COMBINED BYTES IN ARRAY ELEMENT D(J).
21. SEND CONTROLLER LISTEN ADDRESS.
22. SEND 59313A TALK ADDRESS.
23. SEND CHARACTER [1] = SELECT CHANNEL 1.
24. GO THRU LOOP AGAIN.

The array "C" will contain samples from Channel 1 taken at 400 ms intervals (every other pace interval). Array "D" will contain samples from Channel 2 taken at 400 ms intervals and 200 ms later in time than those from Channel 1.

3-45. The final example uses the single conversion mode, the external start, the service request, and conducts a serial poll. The 59313A should have a pushbutton switch on the end of a cable connected to the EXT START jack, or an automatic contact closure associated with the process to be sampled. Each time contact is made, a conversion will take place.

1. SEND UNLISTEN COMMAND [?] .
2. SEND CONTROLLER TALK ADDRESS.
3. SEND 59313A LISTEN ADDRESS [&] .
4. SEND CHARACTERS: [H] RESET.
[8] CHANNEL 4.
[L] SERVICE REQUEST ENABLE.
[A] ONE CONVERSION ONLY.
[K] EXTERNAL START ENABLE.
5. SEND UNLISTEN COMMAND [?] .
6. THE CONTROLLER CAN NOW BE DOING SOME OTHER JOB BUT MUST PERIODICALLY CHECK THE SERVICE REQUEST LINE. IF THE LINE IS INACTIVE, THE OTHER JOB CAN BE PERFORMED BUT IF THE LINE IS ACTIVE THEN A POLL IS CONDUCTED TO SEE WHICH BUS INSTRUMENT IS REQUESTING SERVICE (ASSUMING THERE IS MORE THAN ONE WHICH COULD BE). THEN THE INSTRUMENTS ARE SERVICED.

(PROGRAM CONTINUED)

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POLL:

7. SEND SERIAL POLL ENABLE COMMAND DECIMAL 24 OR OCTAL 30
8. SEND CONTROLLER LISTEN ADDRESS.
9. SEND 59313A TALK ADDRESS F .
10. READ 1 BYTE FROM HP-IB.
11. IF BYTE = 0, 59313A DID NOT REQUEST SERVICE.
IF BYTE = 64, 59313A DID REQUEST SERVICE.
REMEMBER WHICH FOR USE AFTER POLL.
12. SEND OTHER DEVICE TALK ADDRESSES AND READ THEIR BYTES TO
DETERMINE WHICH OF THOSE DEVICES REQUESTED SERVICE.
13. SEND UNTALK COMMAND DECIMAL 95 OR OCTAL 137
14. SEND SERIAL POLL DISABLE COMMAND DECIMAL 25 OCTAL 31
15. IF THE 59313A DID REQUEST SERVICE: (AS INDICATED IN POLL)
 - (a) SEND 59313A TALK ADDRESS F .
 - (b) READ AND COMBINE 2 BYTES FROM HP-IB (SEE PARAGRAPH 3-33).
 - (c) STORE OR USE THE NUMBER AS REQUIRED.
 - (d) SEND 59313A LISTEN ADDRESS & .
 - (e) SEND CONTROLLER TALK ADDRESS.
 - (f) SEND CHARACTER I TO RESET PACER FOR NEXT EXTERNAL START.
 - (g) SEND UNLISTEN COMMAND ? .
 - (h) GO ON TO SERVICE OTHER DEVICES AS REQUIRED.
16. IF THE 59313A DID NOT REQUEST SERVICE JUST GO ON TO SERVICE OTHER
DEVICES AS REQUIRED.
17. GO BACK TO STEP 6.

3-46. Front Panel Controls and Indicators.

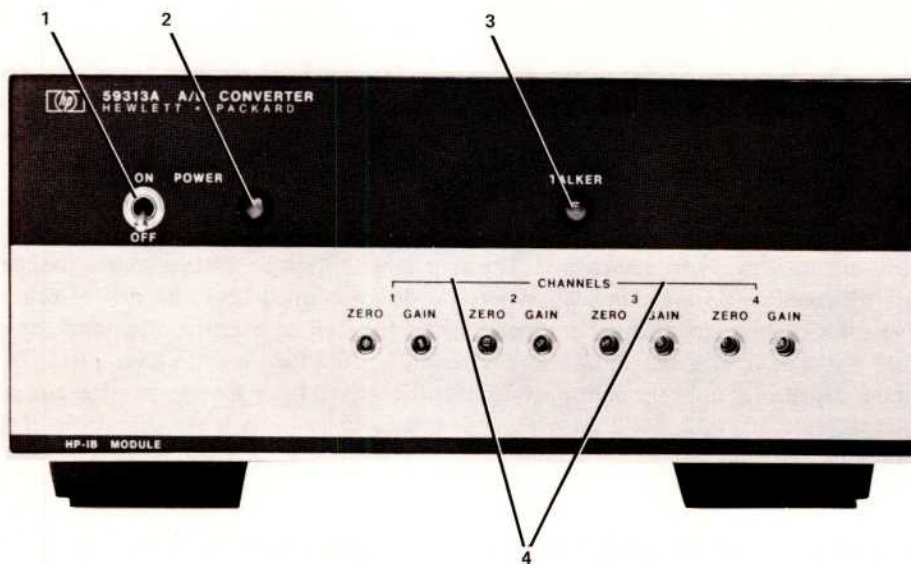
3-47. The front panel controls and indicators are described in Figure 3-7.

3-48. SETTING THE ZERO AND GAIN CONTROLS.

- (a) The ZERO control is adjusted first, then the GAIN control.
- (b) Since there is a slight interaction between the two controls, both adjustments should be repeated if a large gain change is made after setting the zero.

NOTE: For maximum accuracy the 59313A should be warmed up for at least 10 minutes. Operating temperature stabilizes fully in about two hours.

- (c) The HP-IB controller should be programmed with a simple loop to display the output of the 59313A channel to be adjusted (see Paragraph 3-39).
- (d) The range selection jumpers inside the 59313A should have been set previously to accommodate the desired full scale voltage (Figure 2-2).



- 1 **POWER SWITCH:** CONTROLS AC POWER TO THE INSTRUMENT; MUST BE IN ON POSITION FOR OPERATION.
- 2 **POWER ON LAMP:** ILLUMINATES WHEN POWER SWITCH IS ON TO INDICATE THAT POWER IS BEING SUPPLIED.
- 3 **TALKER LAMP:** IS ILLUMINATED WHEN THE 59313A IS ADDRESSED TO TALK AND THE ATN LINE IS NON-ASSERTIVE.
- 4 **ZERO AND GAIN CONTROLS:** PROVIDE INDEPENDENT SCREWDRIVER GAIN TRIM OF ABOUT $\pm 17\%$ AND ZERO TRIM OF ABOUT $\pm 2\%$ FOR EACH OF THE FOUR ANALOG INPUT CHANNELS.

Figure 3-7. 59313A Front Panel

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Model 59313A

(e) With the test program running, apply zero volts to the analog input jack of the channel being tested. Using a small screwdriver, turn that channel's front panel ZERO control until the controller displays zero.

NOTE: For maximum accuracy, try to center the control in the zero region.

(f) Zero volts can be obtained in several ways:

(1) The two wires going to the analog input jack can be shorted together.

(2) The phone plug can be pulled out of the analog input jack and the rear panel CAL switch moved to the "0" position.

(3) The device connected to the analog input jack can have its output go to zero; for example, if an electronic pressure transducer is in use, zero pressure could be applied to its input. This method would also take care of any zero offset appearing on the pressure transducer output or any offset resulting from the 59313A input bias current (100 nA max) interacting with a high output impedance pressure transducer, as ($i_{\text{BIAS}} \times Z_{\text{OUT}} = V_{\text{OFFSET}}$).

(g) There are three ways to adjust gain. The first uses a precision voltage source connected to the analog input jack. This could be a voltage standard where the dials are simply set to the desired voltage or could be a variable power supply with a good digital voltmeter connected to it to monitor the voltage. Simply set the source to the desired full scale voltage and, using a small screwdriver, turn the channel's front panel GAIN control for the channel under adjustment until the controller displays the desired full scale number. Maximum resolution is obtained with a full scale of 1023, 1022 may be more suitable because it is possible to tell if full scale is exceeded, and 1000 as a full scale may be more convenient to think about, and also permits a slight overrange capability.

(h) A second way to adjust gain uses the device connected to the channel as the calibration source. If, for instance, a pressure transducer is in use, a manometer and pressure source could be connected to the transducer and a full scale pressure applied. The front panel GAIN control is then adjusted until the controller displays the full scale value previously selected.

(i) The third way to adjust gain uses the 59313A internal calibration voltage. When the phone plug is removed from the analog input jack of the channel to be adjusted, the calibration voltage is automatically connected. The rear panel CAL switch can then select -1.00 volts or -5.00 volts. -1V is used when a full scale between 1 and 5 volts is desired and -5V is used for a full scale between 5 and 10 volts. If the full scale desired is exactly 1 or 5, the corresponding voltage is selected and the front panel GAIN control turned until the controller displays *negative* full scale. For a full scale of other than 1 or 5 volts, the following formula gives the number the controller must display when the GAIN control is set correctly.

$$N = \frac{\text{OUTPUT} \times V_C}{V_F}$$

where

N = NUMBER DISPLAYED ON CONTROLLER (CALCULATOR)

OUTPUT = DESIRED 59313A FULL SCALE OUTPUT (for example: 1023, 1022, or 1000)

V_C = CALIBRATION VOLTAGE USED (for example: -1 or -5)

V_F = DESIRED FULL SCALE ANALOG INPUT VOLTAGE.

(h) For full scale voltages that lie between the available ranges, for instance 4 volts, the only recourse is to go to the next higher voltage range, 5 volts in this case, and set the gain to produce the highest output possible. This results in some loss of resolution since only part, 4/5 in this case, of the scale is used.

3-49. Reconversion of Output.

3-50. Converting the 59313A output back to the original input units can easily be done by having the controller program multiply each reading by a scale factor K to be determined with the following formula:

$$K = \frac{\text{INPUT FULL SCALE (VOLTS, mmHg, or LITERS/SECOND, etc.)}}{\text{59313A OUTPUT FULL SCALE}}$$

Example 1:

If 3 volts input produces a full scale output of 1022, then $K = 3/1022 = .002935$, so if every reading is multiplied by .002935 before displaying, then the display reads directly in volts.

Example 2:

The pressure transducer produces 10 volts out at a full scale of 80 mmHg. The 59313A has its gain adjusted so this pressure produces a controller display of 1022.

$$K = \frac{80 \text{ mmHg}}{1022} = .07828$$

When each reading is multiplied by this number, the display reads directly in millimeters of mercury.

3-51. Maintaining Resolution.

3-52. Avoid loss of resolution caused by using a scale for convenience's sake. For instance, if a 3-volt full scale is made to produce a 59313A output of 300, 2V = 200, 1V = 100, this would provide only one-third of the resolution obtained by making the 3 volts produce a 59313A output of 1022 and using the K factor described previously.

3-53. Increased Resolution.

3-54. Some devices such as amplifiers designed for use with strip chart recorders may have a provision for obtaining a full scale offset, usually in the negative direction, so that zero is now at the old negative full scale and full scale is at positive full scale. If an amplifier such as this is used with the 59313A, then the resolution will be twice as fine as would otherwise be obtained. Of course, the signals can only swing in one direction from zero and the controller must be programmed to add a constant (e.g. 1022) to each number so the output numbers will run from 0 to +2044 as desired.

NOTES

SECTION IV PRINCIPLES OF OPERATION

4-1. INTRODUCTION.

4-2. This section starts with a block diagram which shows each main functional circuit of the 59313A A/D Converter. Each block is expanded into a block diagram showing key signal lines and main features of that circuit, explained in the text following the diagram. The sequence of block diagrams and text is arranged, generally, so each explanation paves the way for the ones following it. Each block is not confined to one circuit board. Whenever possible, a board designation is provided in the block to aid in troubleshooting on a board-replacement level.

4-3. Mnemonics.





4-4. Some useful notations in this section (and on the schematics) are defined here:

H prefix, examples: H DAC (data accepted)
H DI3 (data in line #3)





indicates the signal line is HI (≈ 3 to 5V) in its assertive or true state.

L prefix, examples: L DAV (data valid)
L DI3 (data-input line #3)

indicates the signal line is LO (0 to 0.4V) in its assertive or true state.

 or  prefix, examples:  PACER TIME MARK
 START CONVERSION

indicates that the rising or falling edge as the line changes state is the event of interest (see Table 4-1).

 or  prefix, examples:  PACE SELECT
 END OF CONVERSION

indicates that a positive or negative pulse is the event of interest (Table 4-1).

N prefix, examples: N DAC (data accepted)
N RFD (ready for data)

indicates *not* or *inverted*.

The N prefix is necessary because the HP-IB (Hewlett-Packard-Interface Bus) lines are defined LO in the assertive or true state. It was therefore necessary to invert the names of the two lines that were naturally HI in their assertive state.

NOTE: Signals on the bus lines are sent assertive (or true) LO i.e, 0 \approx +3V and 1 \approx +0.2V. Inside the 59313A they may be either way as follows:

HDI6 (DATA IN 6) is HI (+3.5 volts) in the assertive state.

LDI6 (DATA IN 6) is LO (+0.2 volts) in the assertive state. (See Figure 4-4.)

U26 – refers to integrated circuit U26.

Bottom board U26 – refers to U26 on the bottom printed circuit board.

U26 (1) – refers to pin 1 of U26.

U15 (8, 9, 10) – refers to pins 8, 9, and 10 of U15 and is used to indicate one of the 4 gates available in that I.C.

NOTE: All connectors and fingers that connect the 3 main P.C. boards are labeled J1 on each board. All lines run to each board even if they are not used there, e.g., J1 (10) is the TLK CLK signal on all the boards. Refer to Table 4-1 for a list of mnemonics and signal polarities.

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Model 59313A

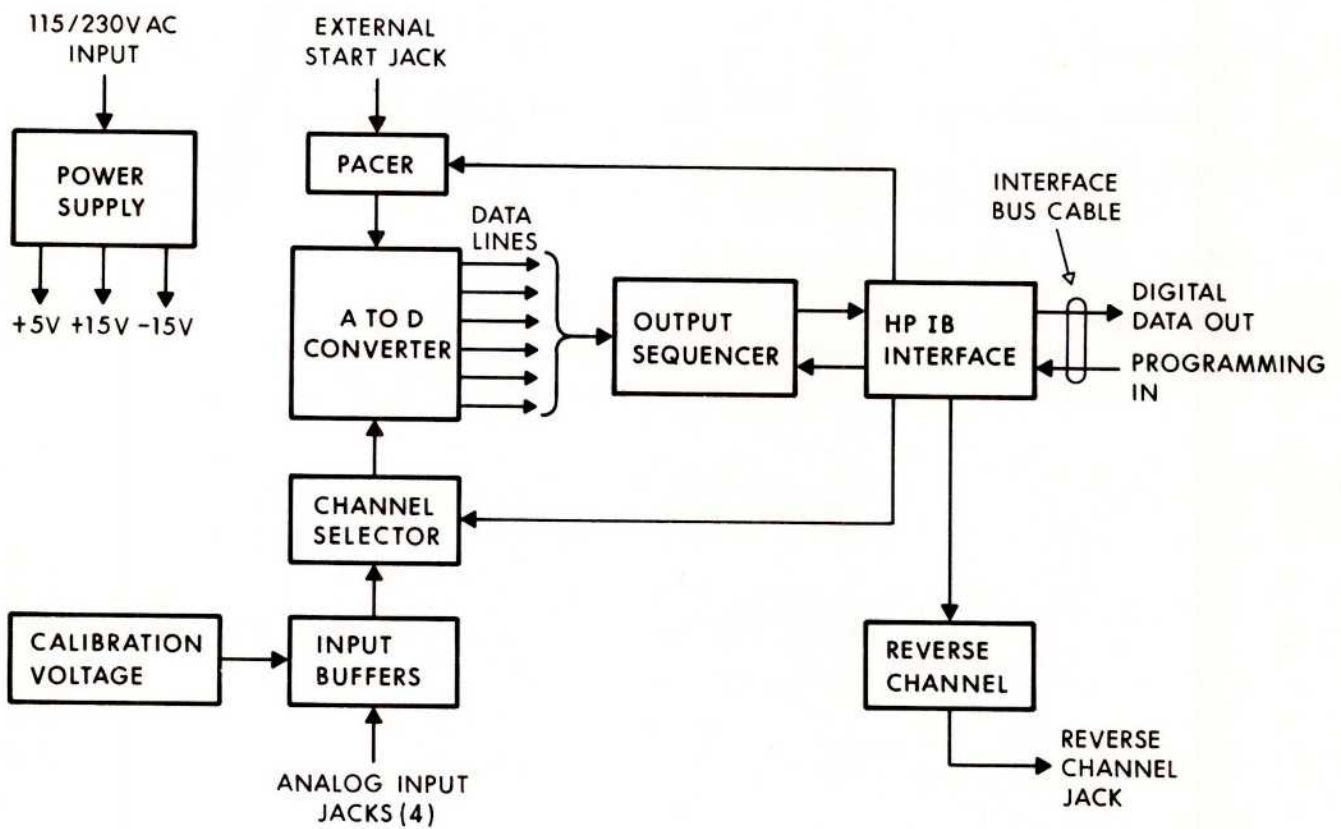
























Figure 4-1. Block Diagram, Model 59313A A/D Converter

Table 4-1. Table of Mnemonics, with Pulse Polarities for Signal Names

<p>The mark  is used to indicate that the rising edge is the event of interest.</p> <p>The mark  is used to indicate that the falling edge is the event of interest.</p> <p>The mark  indicates a positive-pulse is the event of interest.</p> <p>The mark  indicates a negative-pulse is the event of interest.</p>		
Polarity	Mnemonic	Name
L	ATN	ATTENTION
L	LSN	LISTEN
L	NRFD	NOT READY FOR DATA
H	DAV	DATA VALID
	ATN CLK	ATTENTION CLOCK
H	NDAC	NOT DATA ACCEPTED
	LSN CLK	LISTEN CLOCK
L	TLK	TALK
	IFR	INTERFACE RESET
H	DI	DATA INPUT
L	DI	DATA INPUT
L	—	SERIAL POLL MODE
L	—	WAIT FOR INTEGRATOR RESET
L	—	RAMP ACTIVE
H	—	CHANNEL CHANGE INHIBIT
H	—	OUTPUT READY
H	ATN	ATTENTION
H	—	ENABLE SRQ (SERVICE REQUEST)
	SPE	SERIAL POLL ENABLE
H	SRQ	SERVICE REQUEST
	SPD	SERIAL POLL DISABLE
L	—	SERIAL POLL MODE
	RST	RESET
	DCL + POR	DEVICE CLEAR OR POWER-ON RESET
	—	PAGE SELECT
	—	EXTERNAL START ENABLE
	—	PACER TIME MARK
	—	START
	—	START RAMP
H	—	RETURN RAMP
L	—	RAMP ACTIVE
H	—	RUN
	—	START CONVERSION
	—	TM PLUS 4750 μ s
	—	LATCH
	EOC	END OF CONVERSION
	—	REVERSE CHANNEL ON
	—	SELECT ZERO
<p>H indicates HIGH, or about 3 to 5V. L indicates LOW, or about 0 to 0.4V. N indicates not, or inverted.</p>		

4-5. MODES OF OPERATION.

4-6. The 59313A A to D Converter works using four modes of operation; the Attention, Listen, Talk and Serial Poll modes, selected by commands from the HP Interface Bus (Figure 4-2).

4-7. Attention Mode.

4-8. When the bus ATN line is LO the 59313A is in the ATN mode. In ATN, the 59313A interprets the bit patterns on the first 7 DIO (data IN/OUT) lines as a:

- (1) LISTEN address (or UN-LISTEN)
- (2) TALK address (or UN-TALK)
- (3) UNIVERSAL BUS COMMAND

The DIO6 and DIO7 lines determine the category of command or address as follows:

DIO7	DIO6	
0	1	LISTEN
1	0	TALK
0	0	COMMAND

DIO 1 thru 5 then break down each category into 32 individual addresses or commands. The ATN mode has priority over the other three modes and can interrupt and override them at any time.

4-9. Listen Mode.

4-10. If the bus ATN line is HI (non-assertive) and the LLSN line (U26, pin 13, top board) is LO, then the 59313A is in the LSN mode (this happens when the bus controller sends the 59313A's Listen Address.) In LSN, the 59313A interprets the patterns on the first seven DIO lines as control characters, which are arranged in three groups identified by the bit pattern on DIO 4, 5, and 6 as follows:

DIO6	DIO5	DIO4	
0	0	0	PACE SELECT
0	0	1	MISC. CONTROL
1	1		CHANNEL SELECT

4-11. Talk Mode.

4-12. If the bus ATN line is HI (non-assertive) and the L TLK line (U26 (8) top board) is LO, then the 59313A is in the TLK mode and the front panel TALKER lamp is on. (This happens when the bus controller sends the 59313A's Talk Address). In TLK, the 59313A transmits its converter output over the eight DIO lines. The circuitry is arranged so the TLK and LSN modes may not occur simultaneously.

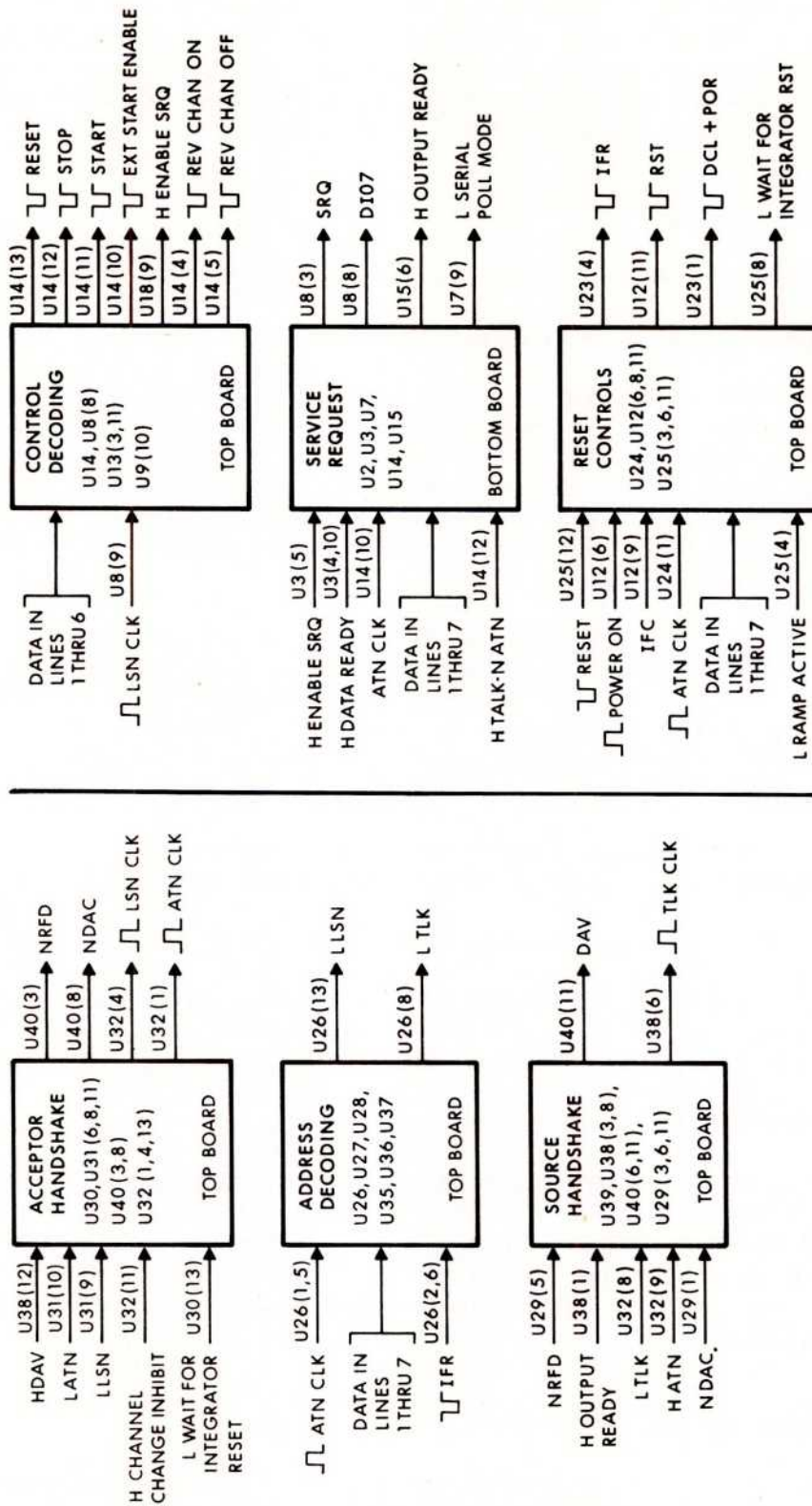


Figure 4-2. Block Diagrams, Interface Bus Connections

Section IV — Principles of Operation
Model 59313A

4-13. Serial Poll Mode.

4-14. If the L SERIAL POLL MODE line (J1, pin 14, from bottom board U7, pin 9) is LO and the ATN line is HI (non-assertive) then the 59313A is in the SERIAL POLL mode. (This happens when the controller sends the Serial Poll Enable command). Serial poll changes the talk mode output from A/D conversion to an output of service request status, so when the TLK address is provided, the 59313A sets DIO7 LO if requesting service and DIO7 HI if *not* requesting service (DIO7 LO = 64).

4-15. LOGIC DESCRIPTION.

4-16. Acceptor Handshake Circuit.

4-17. This circuit operates only in the ATN and LSN modes.

4-18. ATTENTION MODE OPERATION. L ATN line is LO, indicating ATN mode. NRFD (not ready for data) line is HI indicating readiness to accept data. The external bus controller then sets H DAV (data valid) HI (LO on the actual bus line) to indicate there is data on the 8 DATA IN lines. The 59313A then places a two-microsecond pulse on the ATN CLK (attention clock) line to cause the ADDRESS DECODING, RESET CONTROL, and SERVICE REQUEST sections to respond to the data, if appropriate. At the end of the ATN CLK pulse the NDAC (NOT DATA ACCEPTED) line goes HI and the NRFD line goes LO to tell the controller that there is no longer any need to hold data on the DIO lines.

4-19. LISTEN MODE OPERATION. L ATN line is HI AND L LSN line is LO, generating LSN mode. The NRFD line is HI and the NDAC line is LO indicating to the interface bus talker that the 59313A is ready for data. The bus talker then places (or may already have placed) an ASCII character intended for the 59313A onto the DATA IN lines and sets H DAV HI. A two-microsecond LSN CLK pulse then causes the RESET CONTROLS, CONTROL DECODING, PACER, and CHANNEL SELECTOR sections to respond to the data character if appropriate to do so.

At the end of this pulse, NRFD goes LO and NDAC goes HI to signal the bus talker that the data character is no longer needed. The cycle can repeat as many times as necessary to transfer all the needed data characters.

In the LSN mode there are two special cases where this operation is modified.

(1) The L WAIT FOR INTEGRATOR RESET line is LO because the reset character H is on the DATA IN lines and the integrator circuit in the A to D CONVERTER section is in its active region. (J1 (X) L RAMP ACTIVE from bottom board is LO.) Under these conditions NDAC will stay LO and the LSN CLK pulse will go HI and stay HI until the integrator gets reset a maximum of about 2.5 ms later. The L WAIT FOR INTEGRATOR RESET line then goes HI and the cycle completes normally.

(2) The H CHAN CHANGE INHIBIT line goes HI when any channel change character (e.g., 1, 2, 4, 8) is on the DATA IN lines and the A to D CONVERTER section is in the two-millisecond part of its cycle where it is using one of the input channels. Under these conditions the NDAC line stays LO and the LSN CLK pulse is not generated. When the A to D CONVERTER is done with the old channel, the H CHAN CHANGE INHIBIT line goes LO and the cycle completes normally with the generation of the LSN CLK pulse, which will cause the new channel to be selected and NDAC to go HI and NRFD to go LO.

4-20. Address Decoding Circuit.

4-21. This circuit has 5 jumpers (Table 4-2) that program the 59313A to respond to any *one* of the 31 TALK/LISTEN ADDRESS code pairs (sometimes called device I.D. numbers).

Table 4-2. Allowable Address Codes

Address Jumpers					Talk Address Character	Listen Address Character	Device I.D. Code
Data In 5	Data In 4	Data In 3	Data In 2	LSB Data In 1			
0	0	0	0	0	@	SP	0
0	0	0	0	1	A	!	1
0	0	0	1	0	B	"	2
0	0	0	1	1	C	#	3
0	0	1	0	0	D	\$	4
0	0	1	0	1	E	%	5
0	0	1	1	0	F	&	6
0	0	1	1	1	G	' (APOS.)	7
0	1	0	0	0	H	(8
0	1	0	0	1	I)	9
0	1	0	1	0	J	*	10
0	1	0	1	1	K	+	11
0	1	1	0	0	L	, (COMMA)	12
0	1	1	0	1	M	-	13
0	1	1	1	0	N	.	14
0	1	1	1	1	O	/	15
1	0	0	0	0	P	0	16
1	0	0	0	1	Q	1	17
1	0	0	1	0	R	2	18
1	0	0	1	1	S	3	19
1	0	1	0	0	T	4	20
1	0	1	0	1	U	5	21
1	0	1	1	0	V	6	22
1	0	1	1	1	W	7	23
1	1	0	0	0	X	8	24
1	1	0	0	1	Y	9	25
1	1	0	1	0	Z	:	26
1	1	0	1	1	[;	27
1	1	1	0	0	\	<	28
1	1	1	0	1]	=	29
1	1	1	1	0	(>	30

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4-22. ADDRESSING OPERATION. Addressing, which can only be done in the ATN mode, is done as follows:

- (1) A code placed on the DATA IN lines by the bus controller causes generation of an ATN CLK pulse.
- (2) If the code is the LISTEN ADDRESS code selected by the jumpers, then the L LSN line will be latched LO.
- (3) If the code is the TALK ADDRESS code selected by the jumpers, then the L TLK line will be latched LO.

4-23. UNTALK-UNLISTEN OPERATION. The L LSN line can be cleared (set HI) by:

- (1) IFR (INTERFACE RESET) pulse from RESET CONTROL.
- (2) Receiving the UNLISTEN code.
- (3) Receiving the jumper selected TALK ADDRESS.

The L TLK line can be cleared (set HI) by:

- (1) IFR (INTERFACE RESET) pulse from RESET CONTROL.
- (2) Receiving the UNTALK code.
- (3) Receiving the jumper selected LISTEN ADDRESS.
- (4) Receiving any TALK ADDRESS *other than* the jumper-selected one.

TALK and LISTEN cannot occur together. When L TLK is LO, ATN is non-assertive and SERIAL POLL is not in effect, then the 59313A is in the TALK mode. When L LSN is LO and ATN is non-assertive, then the 59313A is in the LISTEN mode.

4-24. Source Handshake Circuit.

4-25. This circuit operates only in the TLK mode (with or without the SERIAL POLL mode). For the handshake to take place two conditions are necessary:

- (1) The 59313A OUTPUT SEQUENCER section must have placed its output data on the 8 DIO lines and set the H OUTPUT READY line HI.
- (2) The bus listener(s) must have set the NRFD line HI and NDAC line LO. Two to four microseconds later the DAV (data valid) line will go LO to indicate to the listener(s) that the data is ready and at the same time TLK CLK goes HI. When the listener(s) have accepted the data they set the NRFD line LO and the NDAC line HI and the source handshake circuit then sets the DAV line HI and the TLK CLK line LO. (The TLK CLK signal is used by the output sequencer to get the next data byte ready.) The source handshake is disabled when either the H ATN or L TLK line goes HI.

4-26. Control Decoding Circuit.

4-27. This section only operates in the LSN (listen) mode. The bus controller puts a control character (Table 4-3) on the DATA IN lines and a two-microsecond (μ s) LSN CLK pulse is sent to this block.

If the character is **H**, a 2μ s, RESET pulse occurs;

if **I**, a 2μ s, STOP pulse occurs;

if **J**, a 2μ s, START pulse occurs;

if **K**, a 2μ s, EXT START ENABLE pulse occurs;

if **L**, H ENABLE SRQ goes HI;

if **M**, H ENABLE SRQ goes LO;

if **N**, a 2μ s, REV CHAN ON pulse occurs;

if **O**, a 2μ s, REV CHAN OFF pulse occurs.

Any other valid 59313A code will cause no output.

Table 4-3. Control Codes

ASCII Character	Data In Code	Control Name
H	X 1 0 0 1 0 0 0	RESET
I	X 1 0 0 1 0 0 1	STOP
J	X 1 0 0 1 0 1 0	START
K	X 1 0 0 1 0 1 1	EXT START ENABLE
L	X 1 0 0 1 1 0 0	SRQ ENABLE
M	X 1 0 0 1 1 0 1	SRQ DISABLE
N	X 1 0 0 1 1 1 0	REV CHAN ON
O	X 1 0 0 1 1 1 1	REV CHAN OFF

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4-28. Service Request Circuit.

4-29. This circuit functions whenever the SERVICE REQUEST feature and/or SERIAL POLL mode is used. The normal sequence of events is as follows:

(1) The H ENABLE SRQ line is set HI by control character **[L]**, which allows the SRQ (SERVICE REQUEST) line to be pulled LO at the end of each conversion when the H DATA READY line goes HI.

(2) When the bus controller senses the SRQ line LO it places the UNIVERSAL BUS COMMAND SPE (SERIAL POLL ENABLE) on the DATA IN lines with the 59313A in the ATN mode.

(3) This generates the two-microsecond ATN CLK pulse, which makes the L SERIAL POLL MODE line go LO because SPE is decoded.

(4) This line LO inhibits the normal operation of the OUTPUT SEQUENCER.

(5) The bus controller then addresses the 59313A as a talker, which makes the H TALK • N ATN line go HI.

(6) This is immediately followed by the SRQ line being cleared (HI, assuming that no other external bus device is also holding it LO) and the DIO7 line being set LO to tell the bus controller that the 59313A had indeed pulled the SRQ line. The controller cannot identify the bus device that pulled the SRQ line LO except by polling (unless there is only one device capable of doing so.)

(7) The H OUTPUT READY line also goes HI at this time to initiate the SOURCE HANDSHAKE which will transfer the status byte to the bus controller.

(8) After the status byte transfer, the controller UNLISTENS the 59313A and may poll some other bus devices by sending their talk addresses.

(9) When the poll, if any, has been completed, the controller places the UNIVERSAL BUS COMMAND SPD (serial poll disable) on the DATA IN lines, ATN CLK occurs, and the L SERIAL POLL MODE lines goes HI. The normal 59313A output is now available if the TLK mode is established.

(10) If the **[L]** SERV REQ ENABLE character has not been sent or a conversion has not been completed, the SRQ line will not be set LO. If the controller conducts a poll under these conditions, the 59313A sets the DIO7 line HI (when addressed to talk) indicating to the controller that it did not request service.

4-30. Reset Controls.

4-31. The 59313A may be reset in one of four ways:

4-32. POWER-ON RESET. When the 59313A power switch is turned on the POWER ON pulse is generated for 1/2 second or so which causes the IFR (interface reset), the RST (reset), and the DCL + POR (device clear or power on reset) pulses to be generated.

4-33. RESET CONTROL CHARACTER **[H]**. When this character is detected by the CONTROL DECODING section (during LSN mode) the 2 μ s duration RESET pulse is generated which in turn generates the RST (reset) pulse. Both pulses hold until the integrator in the A to D CONVERTER section is fully reset (2.5 ms MAX).

The RST pulse clears:

CHANNEL SELECTOR section (no channel selected)

OUTPUT SEQUENCER section (no output)

A to D CONVERTER section (converter cleared)

PACER section (no pace selected)

The REVERSE CHANNEL and the LSN mode are not cleared.

4-34. **DEVICE CLEAR/UNIVERSAL BUS COMMAND.** When the bus controller places the DCL command on the DATA IN lines (during ATN mode) and the ATN CLK pulse is generated, then the IFR, RST, and DCL + POR pulses all occur (the same as power on).

The DCL + POR pulse clears only the REVERSE CHANNEL.

4-35. **INTERFACE CLEAR.** When the bus controller pulses the IFC (interface clear) line LO, the IFR (interface reset) pulse is generated.

The IFR pulse clears the L LSN and L TLK lines of the ADDRESS DECODING section and the L SERIAL POLL MODE line of the SERVICE REQUEST section, i.e., the IFR pulse terminates the TLK, LSN, and SERIAL POLL modes.

4-36. **CIRCUIT DESCRIPTION.**

4-37. Each circuit may not be confined to one circuit board, however, each signal line has the same pin number in each board connector, as shown on the schematic diagram, Figures 6-10, 6-11, and 6-12.

4-38. **Hewlett-Packard Interface Bus (HP-IB) IN/OUT Connections.**

4-39. Each of the HP-IB's 8 DIO (data in/out) lines can transmit data into or out of the 59313A A to D Converter via the bus connector (Figure 4-3). The way one of these lines does this is shown in Figure 4-4.

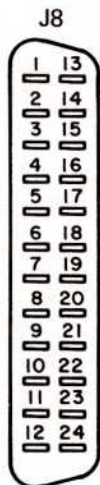
When data is *coming to* the 59313A, the instrument must be in the LSN mode and the open-collector driver on the center pc board is floating. The circuitry then responds only to the HDI5 and LDI5 data input lines. When data is *leaving* the 59313A, the instrument must be in the TALK mode with the center board driver driving the data line DIO5 (data in/out but in this case out only), while the input circuitry ignores the HDI5 and LDI5 lines.

4-40. **Input Buffers (Figure 4-5.).**

4-41. Each of the four analog input channels starts with an operational amplifier connected in the non-inverting mode to present a high impedance to the input signals. Each amplifier's gain can be changed to one of four different levels by a jumper that changes the feedback resistor.

4-42. The GAIN and ZERO POTS control the common summing amplifier (BOTTOM BOARD U27), which follows the input buffer amplifiers. The gain control is part of the input resistance for U27 and thereby varies the stage gain. The zero control adds or subtracts a small constant current to the summing junction (virtual ground) at U27 pin 2 to make the zero offset correction. When the FET switch for the channel is off (open), the controls have no effect. When the phone plug is removed from one of the input jacks, the switching contacts in the jack connect the input to the internal calibration voltage.

MATES WITH
 10631A/B/C
 HP IB CABLE



PIN	LINE NAME	COMMENT
1	DI01	} USED DATA I/O LINES
2	DI02	
3	DI03	
4	DI04	
5	EOI	NOT USED
6	DAV	} USED HANDSHAKE LINES
7	NRFD	
8	NDAC	
9	IFC	} USED
10	SRQ	
11	ATN	
12	SHIELD	NOT CONNECTED
13	DI05	} USED DATA LINES
14	DI06	
15	DI07	
16	DI08	
17	REN	NOT USED
18	GND FOR 6	
19	" "	7
20	" "	8
21	" "	9
22	" "	10
23	" "	11
24	GND FOR OTHERS	

Figure 4-3. Interface Bus Connector Pin Assignments

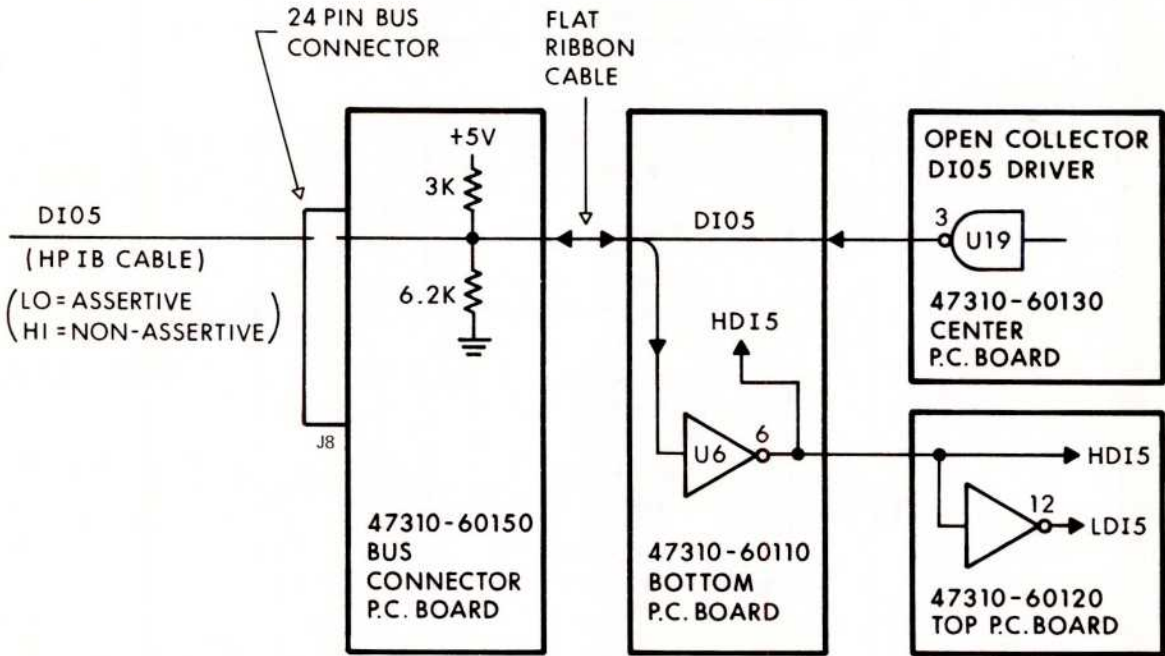


Figure 4-4. Simplified Diagram, Data In/Out Connections

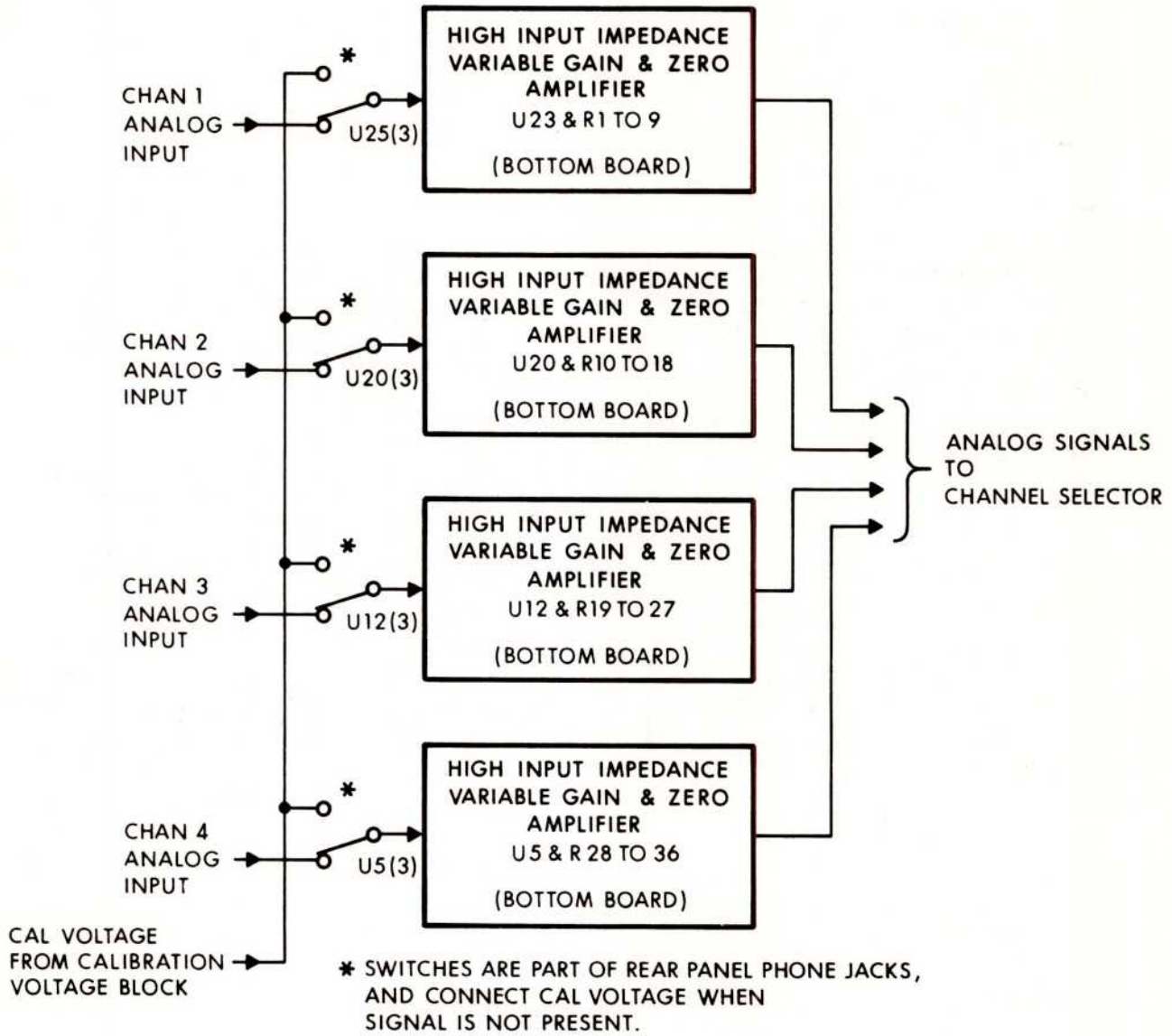


Figure 4-5. Block Diagram, Input Buffers

4-43. Channel Selector.

4-44. The channel selector (Figure 4-6) responds to programming inputs from the calculator to select the channel for data conversion. Selection may be delayed until the preceding conversion is completed.

4-45. ANALOG INPUTS. From an analog signal point of view, a channel is selected when its FET switch is turned on (ON FET ≈ 70 ohms). The signal from that channel then appears inverted at U27 pin 6. The voltage at U27 pin 6 that produces a full scale output from the 59313A is always about ± 9.5 Vdc regardless of which range has been selected. If more than one channel is selected, then the signal at U27 pin 6 is the sum of the individual signals.

4-46. DIGITAL CHANNEL SELECTION. From the digital point of view a channel is selected as follows (Table 4-4): The bus talker places a channel select character on the DATA IN lines while the 59313A is in the LSN (listen) mode and a LSN CLK pulse is generated. If the data character is a channel select character, then the CHANNEL SELECT CHARACTER PREFIX DETECTOR block will detect that DATA IN lines 5 and 6 are both in the TRUE state and the SELECT CHAN pulse is generated. This pulse clocks the 4 flip-flops in the SWITCH CONTROL block which then latch the code present on DATA IN lines 1 thru 4 into their Q outputs. Any Q output that is HI will turn on the FET it is connected to (thru inverter-buffer U17).

Table 4-4. Channel Selection Code

CODE								FET ON	CHAN ON
X	X	1	1	0	0	0	1	Q1	1
X	X	1	1	0	0	1	0	Q2	2
X	X	1	1	0	1	0	0	Q3	3
X	X	1	1	1	0	0	0	Q4	4

The standard channel select characters **1** **2** **4** **8** only turn on one channel at a time and turn off any other that may be on. To turn on more than one channel it is only necessary to select an ASCII code character with the required bits HI. (See ASCII CODE chart, Table 4-7.)

4-47. DELAYED CHANNEL SELECTION. A slight variation to the normal channel selection sequence exists when the A/D CONVERTER section is in the two-millisecond part of its cycle, in which it is using the analog input and has set the H LOOKING AT CHANNEL line HI. This line and the H CHAN PREFIX DETECTED line HI activate the HANDSHAKE INHIBIT block to set the H CHAN CHANGE INHIBIT line HI, which prevents the generation of the LSN CLK pulse by the ACCEPTOR HANDSHAKE block. As soon as the A/D CONVERTER section is through with the analog input, the H LOOKING AT CHANNEL line goes LO, the LSN CLK pulse is generated, and the new channel is selected.

4-48. Pacer.

4-49. The pacer (Figure 4-7) sets the conversion rate, and is programmed from the calculator. These rates include a no conversion choice, one conversion, and automatic pacing from 200 ms to 5 ms intervals.

4-50. INTERVAL GENERATION. The 10 MHz OSCILLATOR and the FREE RUNNING DIVIDER produce a continuous 10-microsecond interval pulse into the RESETTABLE DIVIDER block. The RESETTABLE DIVIDER, when it is not reset, produces 6 pace-interval pulse trains with intervals of 5 ms, 10 ms, 20 ms, 50 ms, 100 ms, and 200 ms which are supplied to the PACE SELECTOR SWITCH block.

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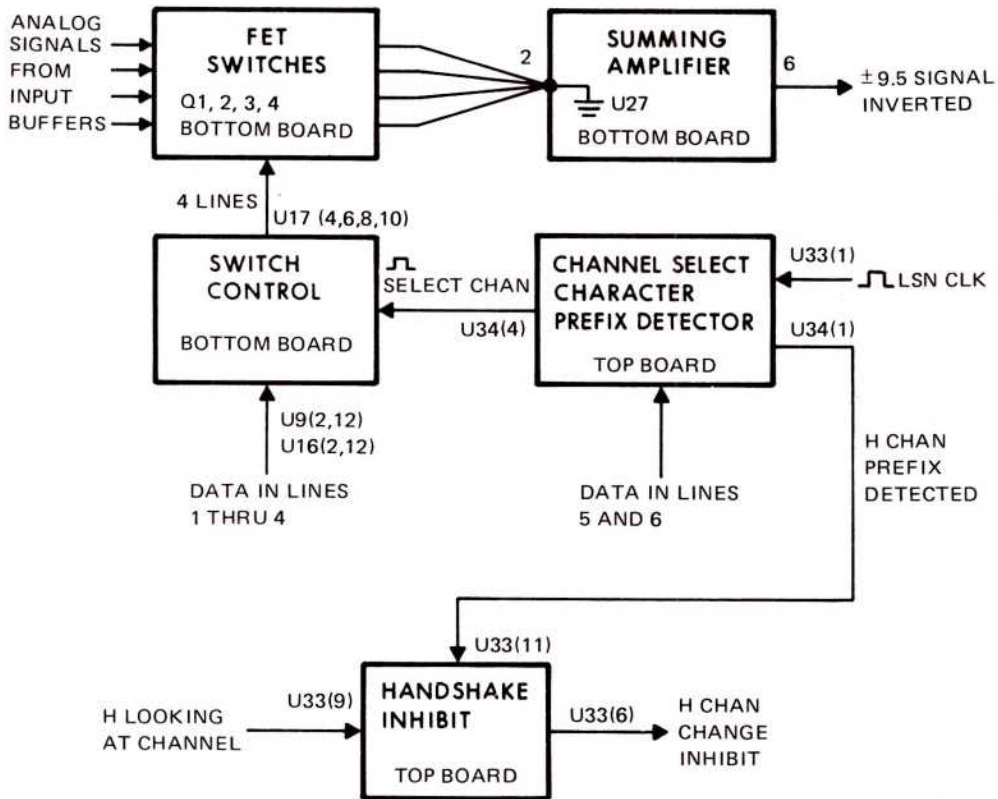


Figure 4-6. Block Diagram, Channel Selector

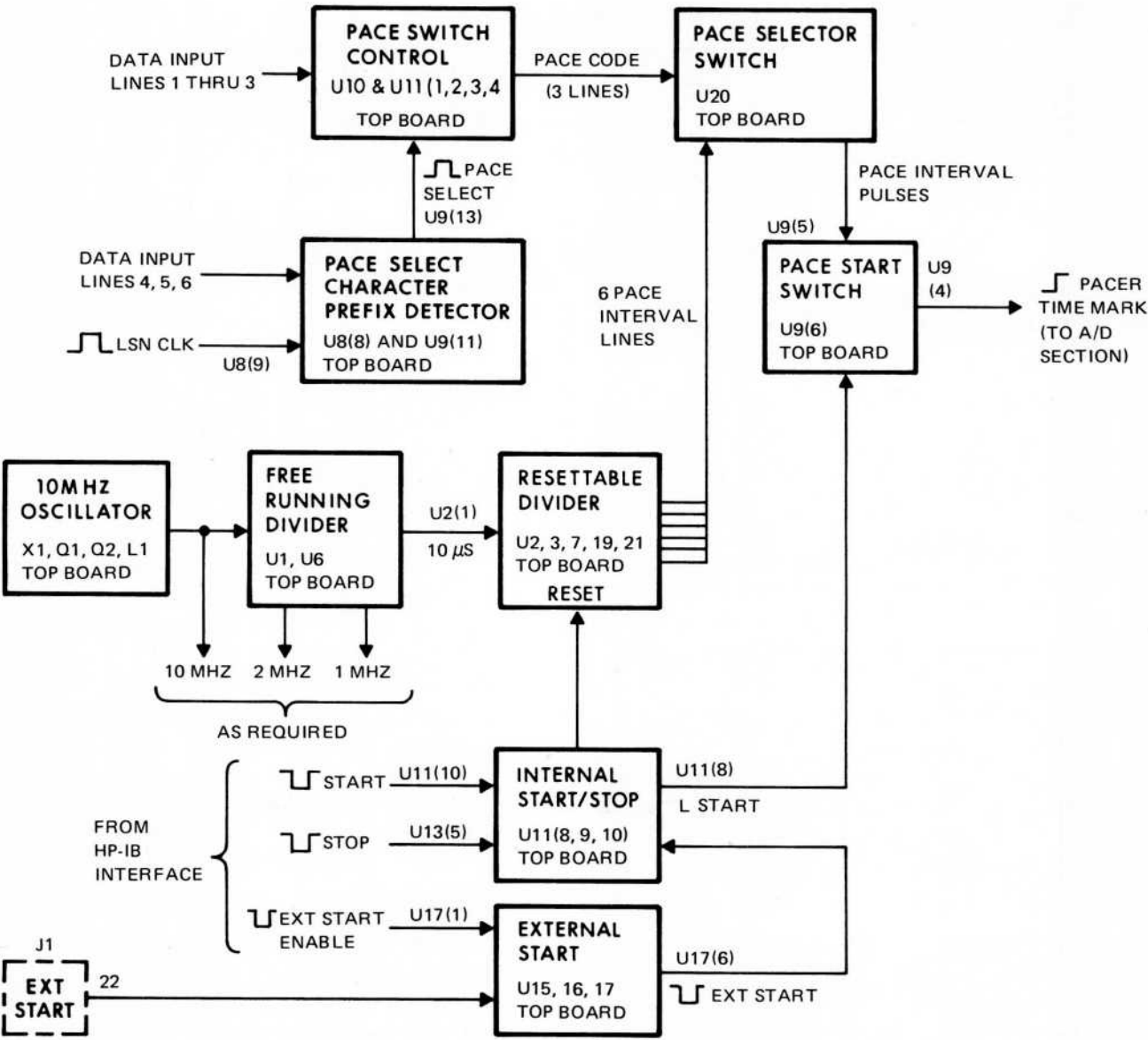


Figure 4-7. Block Diagram, Pacer

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4-51. PACE RATE SELECTION. While the 59313A is in the LSN mode, the bus talker places a pace select character on the DATA IN lines and a LSN CLK pulse is generated. If the character is a pace select character, then the PACE SELECT pulse is generated by the PACE SELECT CHARACTER PREFIX DETECTOR block. The PACE SELECT pulse clocks the 3 flip-flops in the PACE SWITCH CONTROL BLOCK. The Q outputs of these flip-flops then reflect the code on the DATA IN lines 1, 2, 3. The PACE CODE on the Q outputs controls the PACE SELECTOR SWITCH block to select one of the 6 pace intervals supplied by the RESETTABLE DIVIDER block (Table 4-5). The PACE SELECT pulse also goes to the A/D CONVERTER section to blank any false pulses which may be caused by the pace change.

Table 4-5. Pace Selection Codes

Code	Pace Select Character	Pace Interval
X 1 0 0 0 0 0 0	@	None
X 1 0 0 0 0 0 1	A	One Conversion
X 1 0 0 0 0 1 0	B	5 ms
X 1 0 0 0 0 1 1	C	10 ms
X 1 0 0 0 1 0 0	D	20 ms
X 1 0 0 0 1 0 1	E	50 ms
X 1 0 0 0 1 1 0	F	100 ms
X 1 0 0 0 1 1 1	G	200 ms

4-52. INTERNAL START. While the 59313A is in the LSN mode the bus talker sends the START character **J** which generates the START pulse from the CONTROL DECODING section. This sets the INTERNAL START/STOP block L START line HI which enables the PACE START switch block so it can pass the PACE INTERVAL PULSES to the A/D CONVERTER section. At the same time the RESETTABLE DIVIDER block is taken off reset and starts generating its 6 pace interval pulse trains. Whichever of the 6 pace interval pulse trains (or 2 static levels) that is selected by the PACE SELECTOR SWITCH will then appear on the PACER TIME MARK line.

4-53. EXTERNAL START. While the 59313A is in the LSN mode, the bus talker sends the EXT START ENABLE character **K** which generates the EXT START ENABLE pulse from the CONTROL DECODING section. This allows the EXTERNAL START block to respond to the signal from the external start jack. Then when either a LO to HI or a HI to LO transition (a TTL level or contact closure to ground) occurs at the jack, the EXT START pulse is generated. This triggers the INTERNAL START/STOP block to function the same as it does when it gets the START pulse. (See internal start, Paragraph 4-52). The filtering used to prevent false triggering of the external start circuit introduces a typical delay of 0.1 to 2 milliseconds depending on what is used to drive the line.

4-54. PACER STOP. While the 59313A is in the LSN mode the bus talker sends the STOP character **I** which generates the STOP pulse from the CONTROL DECODING section. This causes the INTERNAL START/STOP block to set the L START line LO which disables the PACE START SWITCH and the PACER TIME MARK line. The RESETTABLE DIVIDER is also reset and held there.

4-55. A/D Converter (Figure 4-8).

4-56. The basic dual-slope converter cycle is as follows:

(1) The *unknown* voltage is applied to the input of an integrator for a *fixed* time interval. At the end of the interval the unknown voltage is disconnected and the integrator output remains at some voltage proportional to the unknown.

(2) A *known* reference voltage of opposite polarity is applied to the integrator and the *time* it takes the integrator to return to the starting point is stored in a counter. The stored time is then proportional to the unknown voltage and is the A/D output.

In the A/D CONVERTER description to follow, frequent reference will be made to lines and components on the schematic diagram (Figures 6-10–6-12) that may not appear in the block diagram, Figure 4-8. The timing of the conversion cycle is shown in Figure 4-9.

4-57. ANALOG SIGNAL OFFSET. The $\pm 9.5\text{V}$ SIGNAL INVERTED is scaled and offset by the ANALOG OFFSET AMP block, as in Table 4-6. The output is positive for all inputs. The signal is offset slightly more than that required to make a – (Minus) full scale input coincide with zero volts out. This insures that some + voltage is available for the integrator input for all signal voltages. The error generated by this offset is removed later digitally. When the analog input exceeds the normal full scale range, one of two analog clamps (bottom board U18 and U21) are activated to prevent the ANALOG OFFSET AMP output from exceeding the range of +1.0 to 10.9 volts, which could interfere with integrator operation.

Table 4-6. Offset Amplifier Transfer Functions

Analog Input Signal	$\pm 9.5\text{V}$ Signal (Inverted)	Offset Amp Output (Approx.)
+ Over-Range	–10 to –14V	+10.9V
+ Full Scale	–9.5V	+10.7V
Zero	0V	+5.9V
– Full Scale	+9.5V	+1.2V
– Over-Range	+10 to +14V	+1.0V

4-58. STARTING THE CONVERSION. A PACER TIME MARK edge to U2 pin 11 generates the START CONVERSION edge to U1(5) which sets the H RUN/L RST line HI. This sets the L START RAMP/H RETURN RAMP line HI at U3 pin 3, which causes bottom board Q7 to turn on, thereby connecting the analog input signal to the integrator, U11. This line also turns Q6 and Q8 off (open) so the integrator is no longer clamped to +30 mV. The integrator output now starts moving in the negative direction towards zero volts. The time it takes the integrator to get to zero varies with the signal voltage (Figure 4-10).

4-59. FIXED 2048-MICROSECOND TIME INTERVAL. As the INTEGRATOR crosses zero volts, the COMPARATOR (bottom board U10) switches state and the L RAMP ACTIVE line goes LO to signal the start of the 2048-microsecond fixed time interval. At this time, RAMP ACTIVE 1 MICROSECOND CLOCK pulses start coming from top board U5(9) to center board U17(11) which passes them to the counters (U10, U16, and U22). 2048 pulses later, middle board U4(1) gets clocked, signalling the end of the fixed time interval. The integrator output is now at some voltage proportional to the analog input voltage.

4-60. OFFSET SUBTRACTION. The clocking of U4(1) sets the H START RAMP/L RETURN RAMP line LO which turns bottom board Q7 off and Q6 on, thereby connecting the –9.5 volt reference to the integrator, U11. The output of U11 then moves in the positive direction, towards zero.

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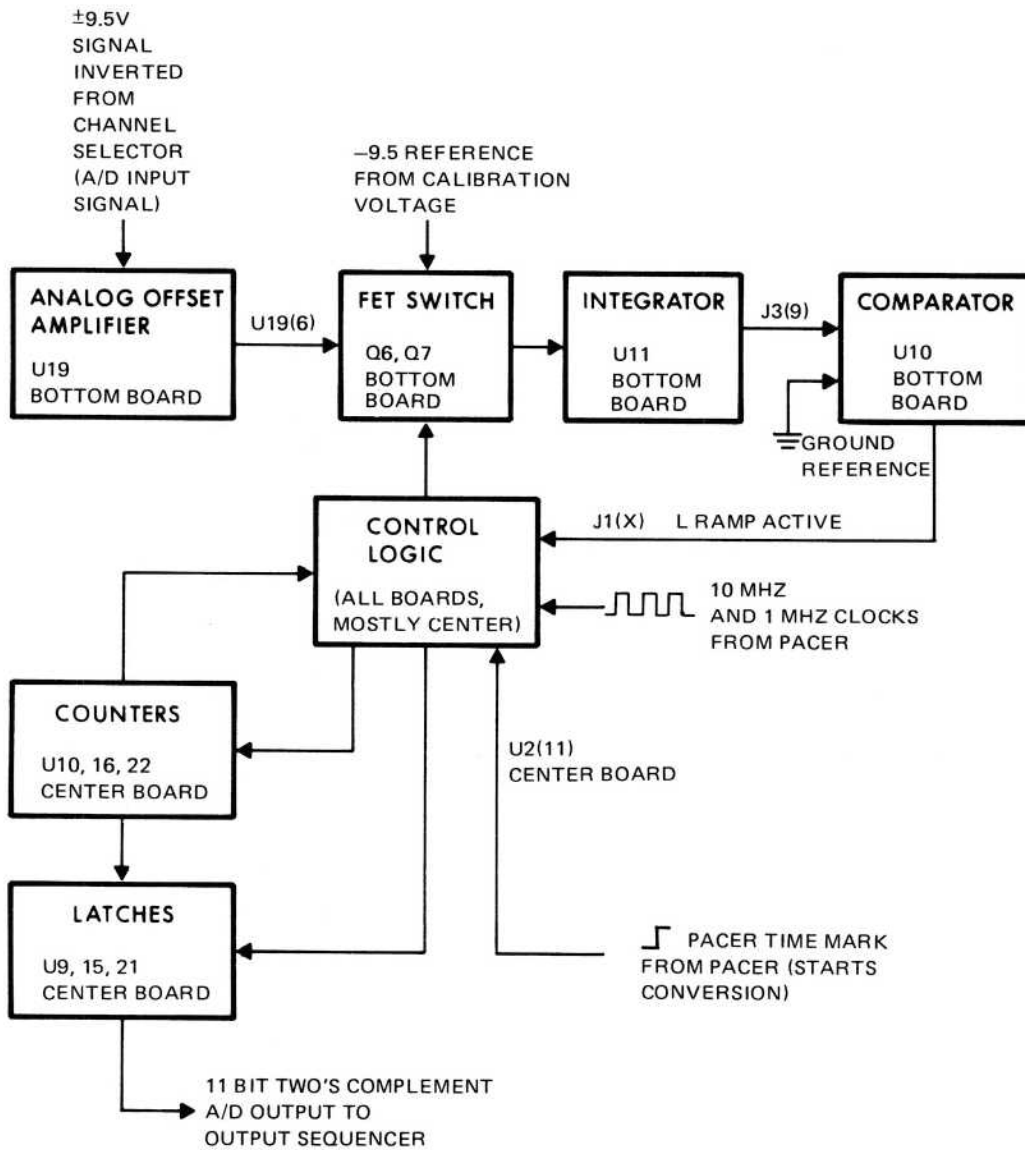
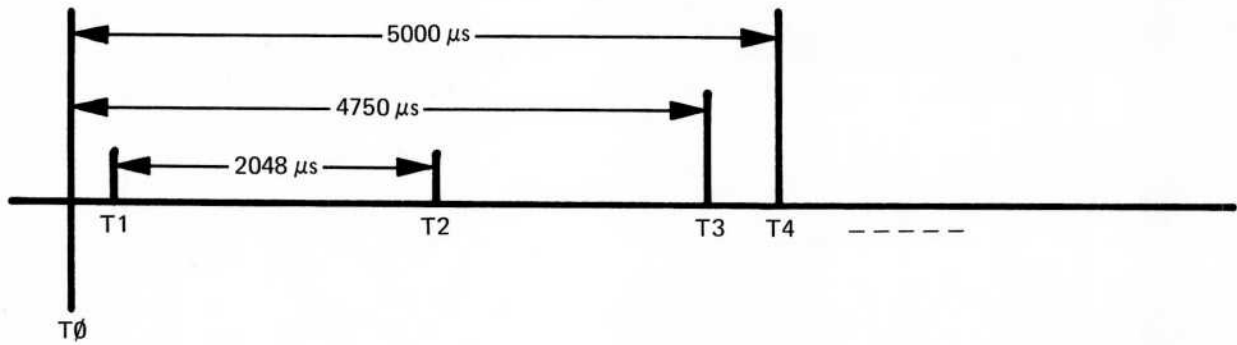


Figure 4-8. Block Diagram, A/D Converter



T_0 IS START-CONVERSION SIGNAL FROM PACER.

T_1 - T_0 IS START UP DELAY (SEE GRAPH IN FIGURE 4-10).

T_2 - T_1 IS TIME INPUT IS NEEDED FOR CONVERSION, CHANNEL SWITCHING IS LOCKED OUT, COMMAND WILL HOLD AT CHANNEL SWITCH CHARACTER.

T_3 , OUTPUT FOR PRESENT CONVERSION BECOMES AVAILABLE AND REMAINS AVAILABLE FOR OUTPUT UNTIL NEXT T_3 .

T_4 , START OF NEXT CONVERSION IF PACER IS SET FOR 5 ms; T_4 EXTENDS TO 10, 20, 50 ms, ETC. IF PACER IS SET TO 10, 20, 50 ms ETC.

SRQ LINE IS PULLED AT T_3 (IF ENABLED).

CHANNEL SWITCHING SHOULD BE DONE $> 100 \mu s$ BEFORE T_0 .

Figure 4-9. Timing Diagram, Conversion Cycle

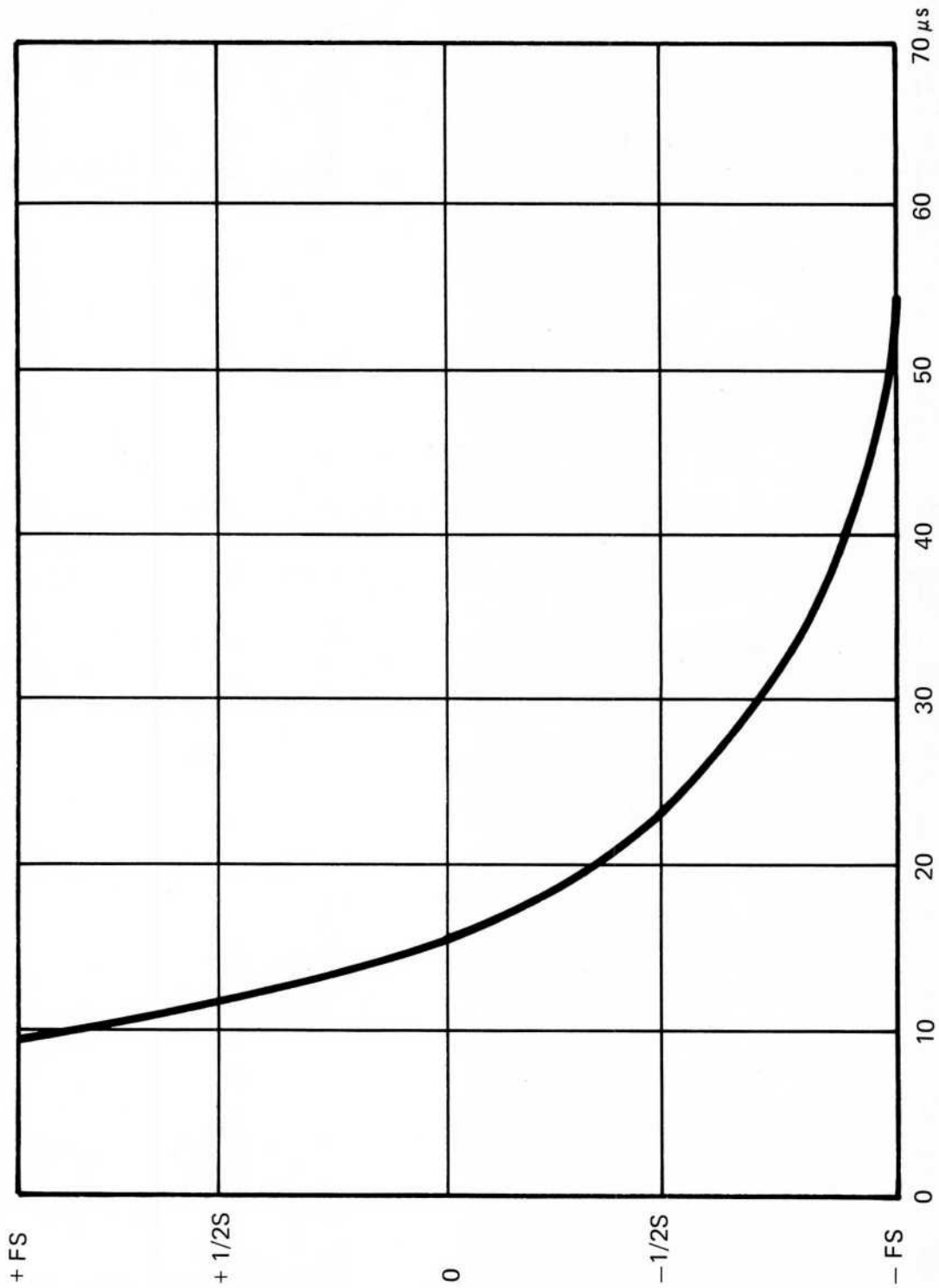


Figure 4-10. Graph, Start-up Delay vs Input Voltage

4-61. Also at this time pin 7 of center board counter U10 goes LO to inhibit that section of the counter. The 11 bits of the counter that are used are all LO now. The first two counter sections, U16 and U22, continue to count until 256 counts (microseconds) later, J4(5) is clocked. The 11 used counter bits are again at all zeros and the 256 counts have been lost to compensate for the extra analog positive offset mentioned previously.

4-62. INTEGRATOR COUNTDOWN. The clocking of U4(5) makes counter U10 pin 7 HI again so the whole counter can count at the 1 MHz rate until the integrator returns to zero. When the integrator gets to zero, the comparator switches state and the L RAMP ACTIVE line goes HI, signalling the end of the counting. The RAMP ACTIVE 1 MICROSECOND CLOCK pulses now stop and the static counters contain the A/D output. Top board U18 (2, 3, 6) and U9 (1, 2, 3) insure that the last pulse is of sufficient duration to properly clock the counters. The L RAMP ACTIVE line being HI also turns on FET Q7 (bottom board) which clamps the integrator at +30 mV. The -9.5V is still on thru Q6.

4-63. END OF CONVERSION. During the last half of the 2048-microsecond fixed time interval, center board flip-flop U1 was reset at pin 2, which reset U6 (decoder U7 was blanked during this reset to prevent unwanted output spikes). All the events mentioned so far are always complete prior to the TM PLUS 4750-MICROSECONDS edge which clocks center board U1 4750 microseconds after PACER TIME MARK initiated the conversion. U6 then comes off reset and starts counting which generates first the LATCH pulse at U7(6) to latch the counters output into the LATCHES (U15, U21, U9) and then the EOC (end of conversion) pulse of U7(8) which resets the counters, and flip-flops U2(10), U1(6), U4(2), and U4(6) thereby preparing the circuitry for another conversion cycle.

4-64. One small variation to the cycle exists when the HALF-OUTPUT INHIBIT line is LO indicating that only one of the two output bytes from the previous conversion cycle has been produced. Under this condition, the LATCH pulse does not reach the latches and the current conversion is not transferred to the latches.

4-65. NEGATIVE OVERRANGE OPERATION. If the analog input voltage is more negative than negative full scale then the integrator gets back to zero during the extra offset subtraction and the center board U5(4) goes HI. The counters are then held reset for the remainder of the cycle and the digital output is clamped to negative full scale.

$$1\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0 = \text{neg full scale} = -1024$$

Sign bit is taken from Q output so is inverted.

4-66. POSITIVE OVERRANGE OPERATION. If the analog input voltage is more positive than positive full scale, then the integrator will not get back to zero before the counters overflow. When they try to overflow U10(15) goes HI which inhibits additional clock pulses to the counters, the outputs then remain at all ones for the remainder of the cycle and the digital output is clamped to positive full scale.

$$0\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1 = \text{pos full scale} = +1023$$

Sign bit is taken from Q output so is inverted. (See Appendix IV for two's complement conversion.)

4-67. Output Sequencer (Figure 4-11).

4-68. In a normal operating sequence the END OF CONVERSION pulse resets the output sequencer flip-flop which sets the L SELECT 0 line LO which directs the byte selector circuit to select the 3 most significant bits of the 11 bit A to D CONVERTER output (the other 5 bits of the 8 bit byte are all tied to the most significant bit, that is, the sign bit). Also at this time the H DATA READY line goes HI to signal the source handshake circuit that the output is ready. As soon as the 59313A is in the TLK mode the H TALK • N ATN line goes HI and this first byte is placed on the 8 DIO (data in/out) lines of the bus. When the bus listener has accepted the byte the

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 Model 593131A

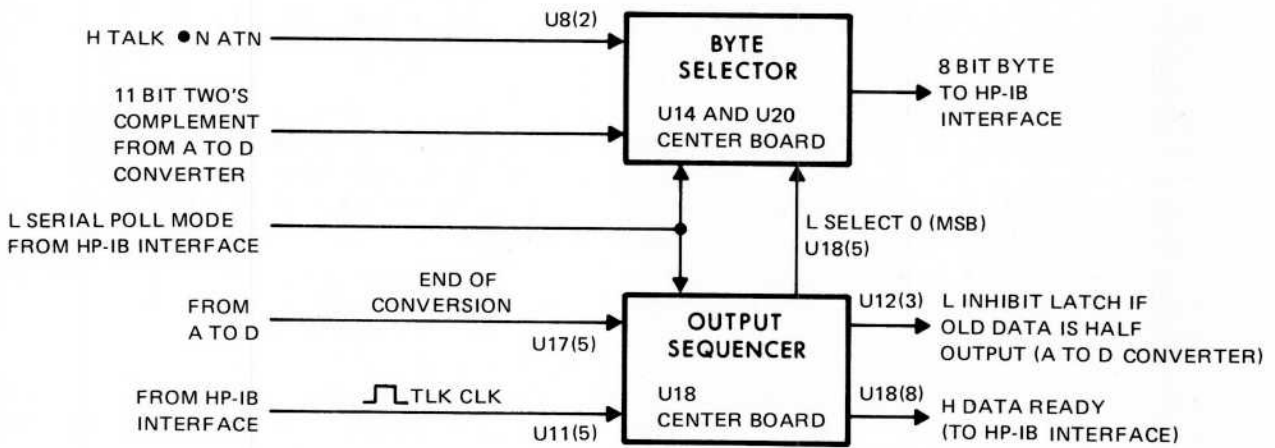


Figure 4-11. Block Diagram, Output Sequencer

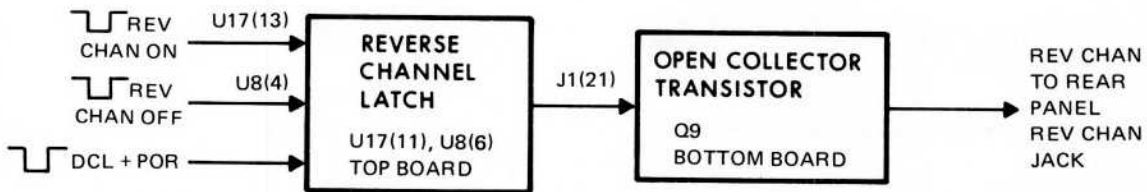


Figure 4-12. Block Diagram, Reverse Channel

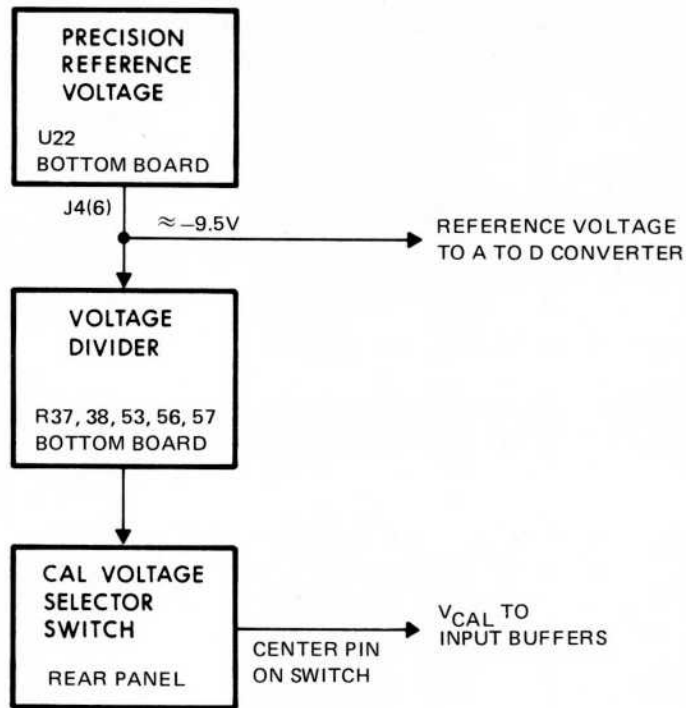


Figure 4-13. Block Diagram, Calibration Voltage

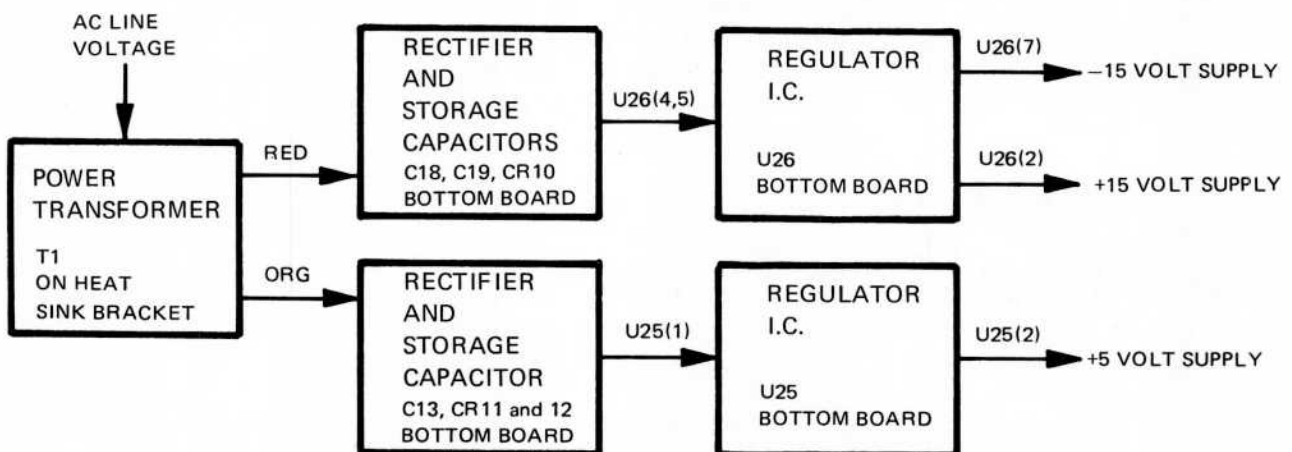


Figure 4-14. Block Diagram, Power Supply

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Model 59313A

source handshake circuit completes the TLK CLK pulse which makes the L SELECT 0 line go HI. The BYTE SELECTOR circuit then places the second 8 bit byte (consisting of the 8 *least* significant bits) on the bus DIO lines. Again, the TLK CLK pulse is generated and the H DATA READY line goes LO so no more bytes can be output until the next conversion is done and the sequence is repeated. Between the first and second bytes the HALF-OUTPUT INHIBIT line is LO so no new conversion data is available until all the old is transferred out. If neither of the two bytes is transferred, then the new conversion data will replace the old.

4-69. If the 59313A is in the SERIAL POLL mode, then the L SERIAL POLL MODE line is LO, the byte selector circuit is disabled (the open collector DIO line drivers are all floating), and the output sequencer circuit ignores the TLK CLK pulse.

4-70. Reverse Channel (Figure 4-12).

4-71. When the 59313A is in the LSN (listen) mode the bus talker sends the ASCII character N which causes the control decoding section to generate the REV CHAN ON pulse which sets J1(21) HI and TRANSISTOR Q9 saturates, grounding the REV CHAN line.

When the ASCII character O (the letter O) is received, the REV CHAN OFF pulse is generated, J1(21) goes LO, transistor Q9 turns off and the REV CHAN line is floating. The DCL+POR (device clear or power on reset) pulse also sets J1(21) LO at power on or when the universal bus command device clear is received (see Paragraph 4-34) thereby turning off Q9.

4-72. Calibration Voltage.

4-73. The precision reference voltage circuit generates a stable approximately -9.5 volts at its output. This -9.5 volts feeds the voltage divider, a resistive divider chain. The cal voltage selector switch changes the cal voltage by shorting the output to ground for zero volts, by shorting out some of the resistors for the -5 volt cal, and by leaving all the resistors in the string for the -1 volt cal. The input buffers that the cal voltage gets connected to thru the input jacks have a high enough input impedance and a low enough bias current so they do not load down the divider chain.

4-74. The calibration voltage is provided as a convenient means to set the individual channel gains and is not intended to be a voltage standard. If absolute accuracy is essential, some external calibration references should be used. Because the cal voltage is derived from the A/D CONVERTER -9.5 reference voltage, the converter output will not show a gain change if the -9.5 changes and the cal voltage is used for calibration.

4-75. Power Supply (Figure 4-14).

4-76. The power transformer takes the 115 volt (primaries in series) or 230 volt (primaries in parallel) ac line voltage and converts it to about 19 Vrms on the RED wire secondary (RED to center TAP) and to about 10-1/2 Vrms on the ORG wire secondary (ORG to center tap). The transformer has internal non-replaceable 103°C thermal cutouts in the primaries.

4-77. +5V SUPPLY. The 10-1/2V from the ORG secondary is full-wave rectified and stored between ac cycles by the rectifier and storage capacitor to produce an average of about +12V. The REGULATOR I.C. takes the high ripple +12 and regulates it to almost ripple free +5 volts. The regulator I.C. also provides current limiting so accidental short circuits do not damage the circuit. Excess heat generated by the I.C. is dissipated into the heat sink bracket.

4-78. $\pm 5V$ SUPPLY. The 10-1/2V from the ORG secondary is full-wave rectified and stored between ac cycles the rectifier and storage capacitors to produce an average of $\pm 25V$. The regulator I.C. takes the high-ripple $\pm 25V$ and regulates it to almost ripple free ± 15 volts. The regulator I.C. also provides current limiting so accidental short circuits do not damage the circuit. Excess heat generated by the I.C. is dissipated into the heat sink bracket.

Table 4-7. Interface Bus Code Set

ASCII CODES
(AMERICAN STANDARD CODE FOR INFORMATION INTERCHANGE)

BITS				b ₇ →	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
b ₄ ↓	b ₃ ↓	b ₂ ↓	b ₁ ↓	COLUMN →	0	1	2	3	4	5	6	7
				↓ ROW								
0	0	0	0	0	NUL	DLE	SP	Ø	@	P	•	p
0	0	0	1	1	SOH	DC1	!	1	A	Q	a	q
0	0	1	0	2	STX	DC2	"	2	B	R	b	r
0	0	1	1	3	ETX	DC3	=	3	C	S	c	s
0	1	0	0	4	EOT	DC4	\$	4	D	T	d	t
0	1	0	1	5	ENQ	NAK	%	5	E	U	e	u
0	1	1	0	6	ACK	SYN	&	6	F	V	f	v
0	1	1	1	7	BEL	ETB	•	7	G	W	g	w
1	0	0	0	8	BS	CAN	(8	H	X	h	x
1	0	0	1	9	HT	EM)	9	I	Y	i	y
1	0	1	0	10	LF	SUB	*	:	J	Z	j	z
1	0	1	1	11	VT	ESC	+	;	K		k	{
1	1	0	0	12	FF	FS	,	<	L	\	l	:
1	1	0	1	13	CR	GS	-	=	M		m	}
1	1	1	0	14	SO	RS	.	>	N	-	n	~
1	1	1	1	15	SI	US	/	?	O	—	o	DEL

ADDRESS MODE

UNIVERSAL COMMANDS UNLISTEN COMMAND UNTALK COMMAND NOT USED

LISTEN ADDRESS TALK ADDRESS

DATA MODE

NOT USED EXCEPT CR, LF AS WORD TERMINATORS ALL DATA NOT USED

NOTES

SECTION V MAINTENANCE

5-1. INTRODUCTION.

5-2. This section contains maintenance and service information, including a table of recommended test equipment, a minimum performance check, adjustments, and troubleshooting procedures.

5-3. Test Equipment.

5-4. Table 5-1 lists the test equipment recommended for maintaining and checking the performance of the 59313A. Test equipment having equivalent characteristics may be substituted for the equipment listed.

5-5. Disassembly.

5-6. The Model 59313A A/D Converter may be disassembled as follows (Figure 5-1):

- a. Remove the top, bottom, and left side covers.
- b. (1) Remove four screws (A) securing the upper board assembly.
(2) By the transformer there is a place (B) where the forefinger can reach under both Top and Middle circuit boards. Pull up with the finger, thereby disengaging the connector.
- c. (1) Carefully remove the eight wires attached to the four input cables (C) from the pc board pins, the four power and talker lamp wires across the front of the lower board (D), and the six external-start, calibration switch, and ground wires along the rear of the board (E).
(2) Remove plugs P6 and P8 connected to the rear of the board.
- d. Stand the instrument on its left side (transformer up), and remove five screws designated (F).
- e. Stand the instrument on its right side (transformer down).
(1) Remove two screws (G) from the top of the board.
(2) Remove two screws (H) from the bottom of the board.
(3) Remove two screws (I) holding the transformer.
(4) Remove one screw (J) holding the primary power cable.
(5) Swing the transformer out of the instrument (Figure 5-1, part 6), and rest it on the table surface, making sure that the primary wires are not pulled or broken.
- f. With the instrument on its left side again, and with the component side of the pc board facing you:
(1) Grasp the right screw tab (K) with your right hand.
(2) Reach around and grasp the left lower edge of the pc board from behind (L).
(3) Lifting up on the tab and pc board, slide the board to the left.

Table 5-1. Recommended Test Equipment

Instrument	Characteristics	Suggested Model No.
Digital Voltmeter	5 Digit Display 0 to ±15 Vdc 4-1/2 Digital Display 0 to ±15 Vdc	HP 3490A — for any check HP 3480 — for any check except linearity
Logic Probe	Low-Power TTL Compatible	HP 10525T
HP-IB Controller	Send ASCII over bus. Receive and manipulate binary. Display or print numbers.	HP 9815A } desktop HP 9820A } calculator HP 9825A } w/HP-IB HP 9830A } interface
Variable Voltage	200 μV resolution 0 to 20 volts (floating)	HP 6111A Power Supply
Frequency Counter	Period function 5 ms to 200 ms	HP 5300A/5302A

(4) Pulling on the right tab, angle the right side of the board, making sure the ZERO and GAIN potentiometers and pc board edge clear the front panel bushings.

(5) Slide the board to the right and, while lifting on the tab and pc board, angle the left edge of the board away from you and out of the instrument, making sure the heat sink clears the side casting and the primary power cable clears the two screw tabs.

g. Install the replacement board by reversing the disassembly procedure.

5-7. MINIMUM PERFORMANCE CHECK.

5-8. Preliminary Setup.

5-9. No warm-up period is required to perform these performance checks. Before applying power, verify that:

- (1) The rear panel voltage selector (115/230) switch is in the correct position (Figure 2-1).
- (2) A fuse of the correct rating is in the rear panel fuse holder (Figure 2-1).

5-10. For the standard HP-IB sequences required to send an address, a universal bus command, or a control character (Table 5-2), refer to the controller manual(s) for details on how to achieve these standard HP-IB sequences. With most controllers (Table 5-1) the handshake and the ATN line are taken care of without the knowledge of the operator.

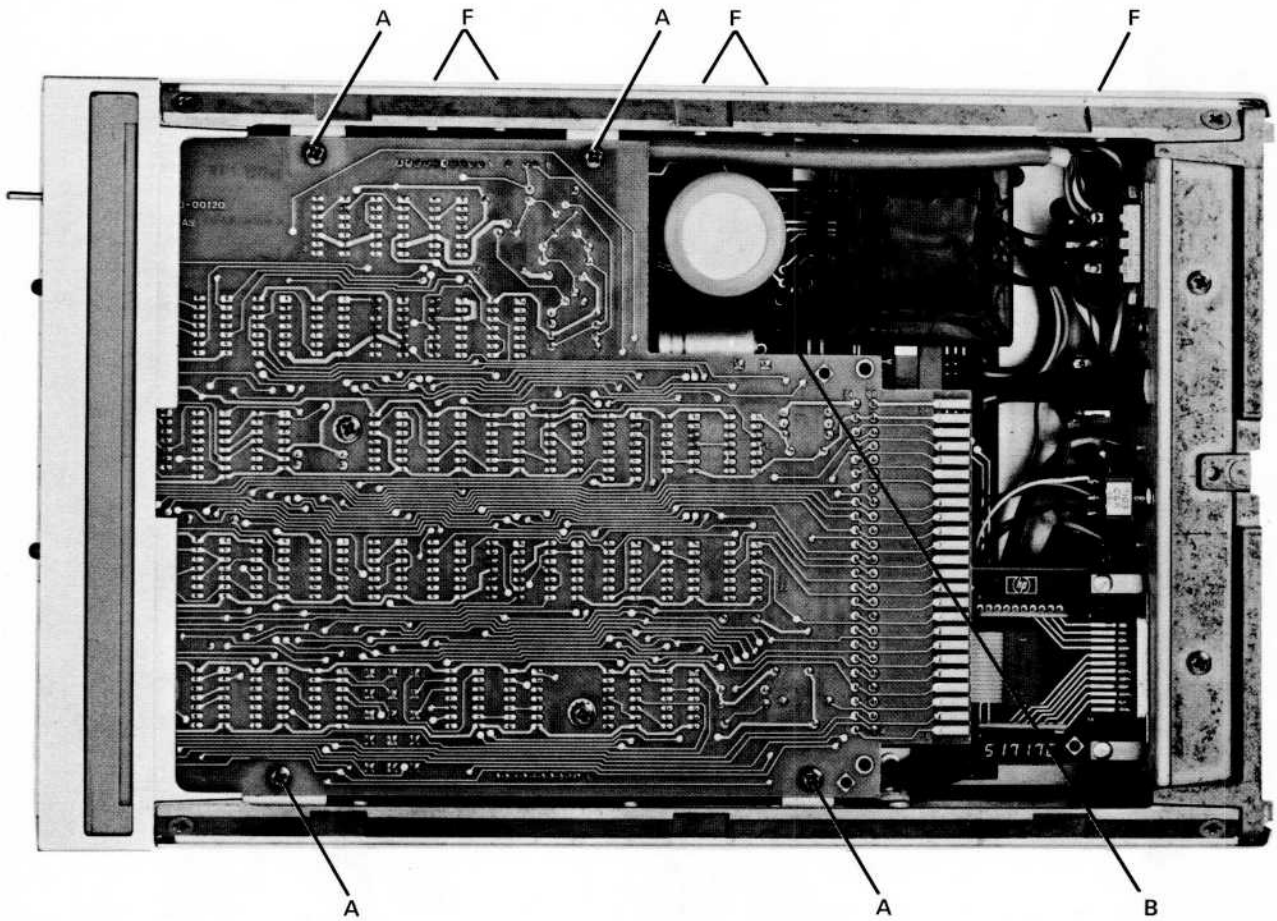


Figure 5-1. Disassembly (1 of 6)

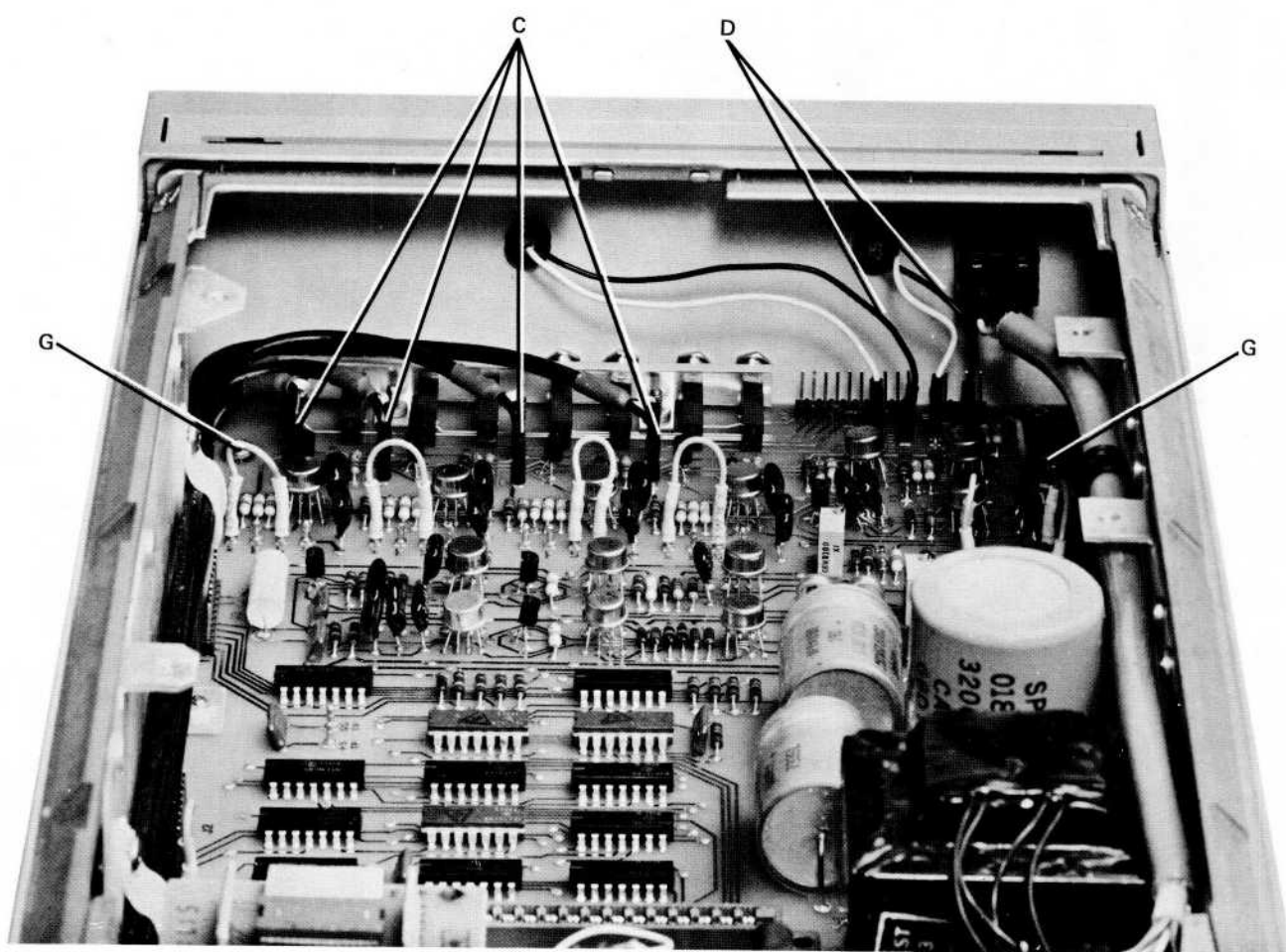


Figure 5-1. Disassembly (2 of 6)

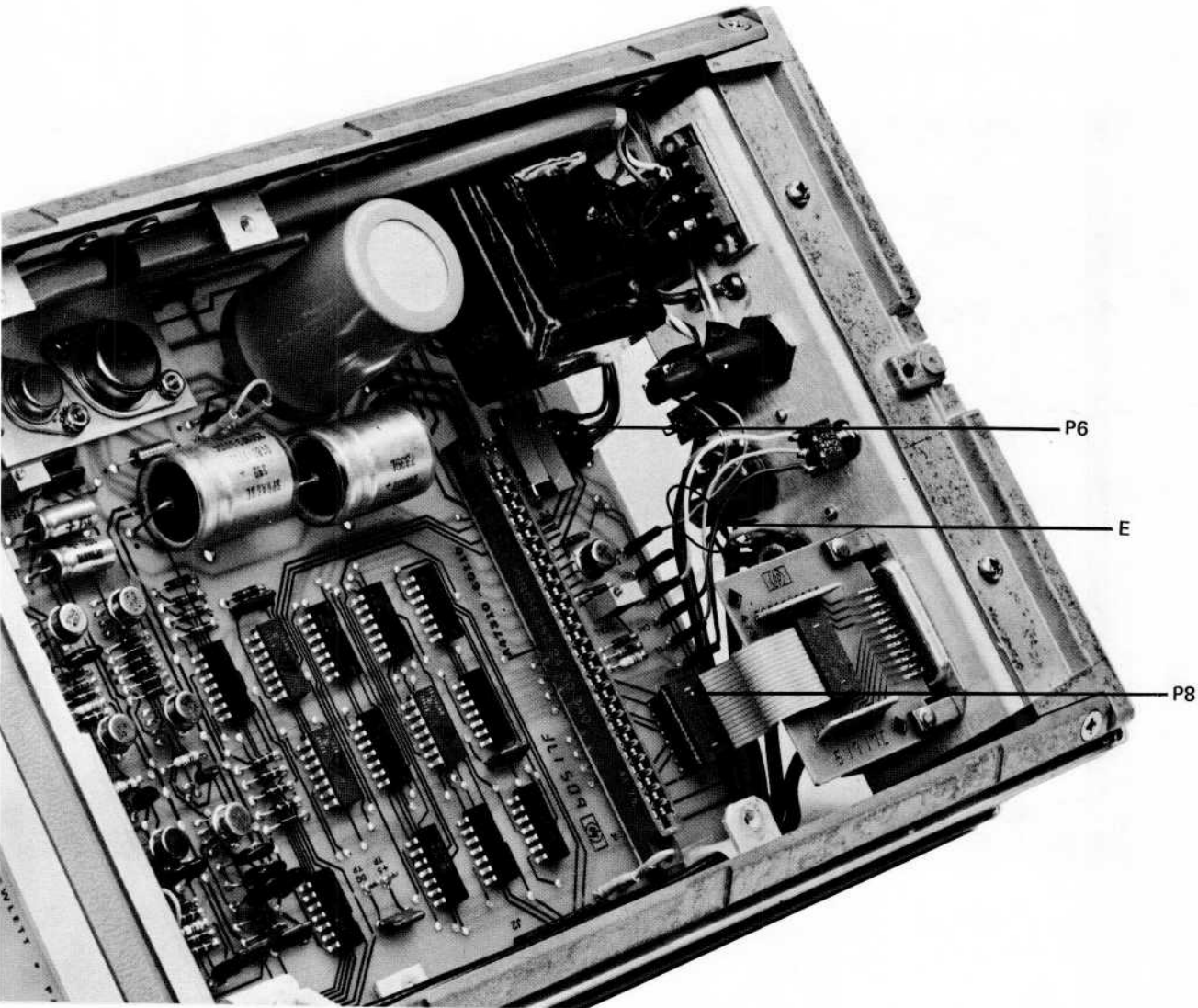


Figure 5-1. Disassembly (3 of 6)

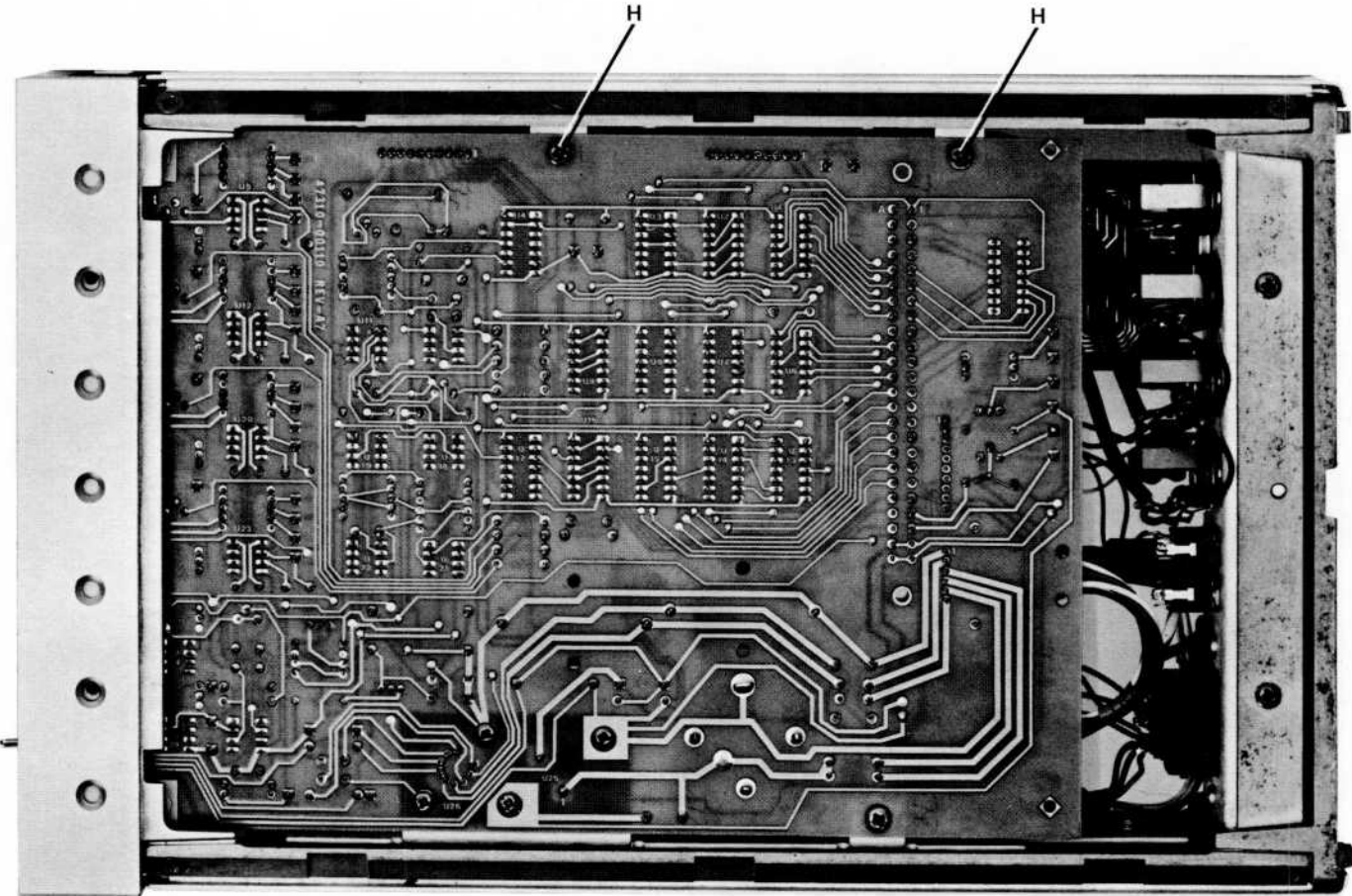


Figure 5-1. Disassembly (4 of 6)

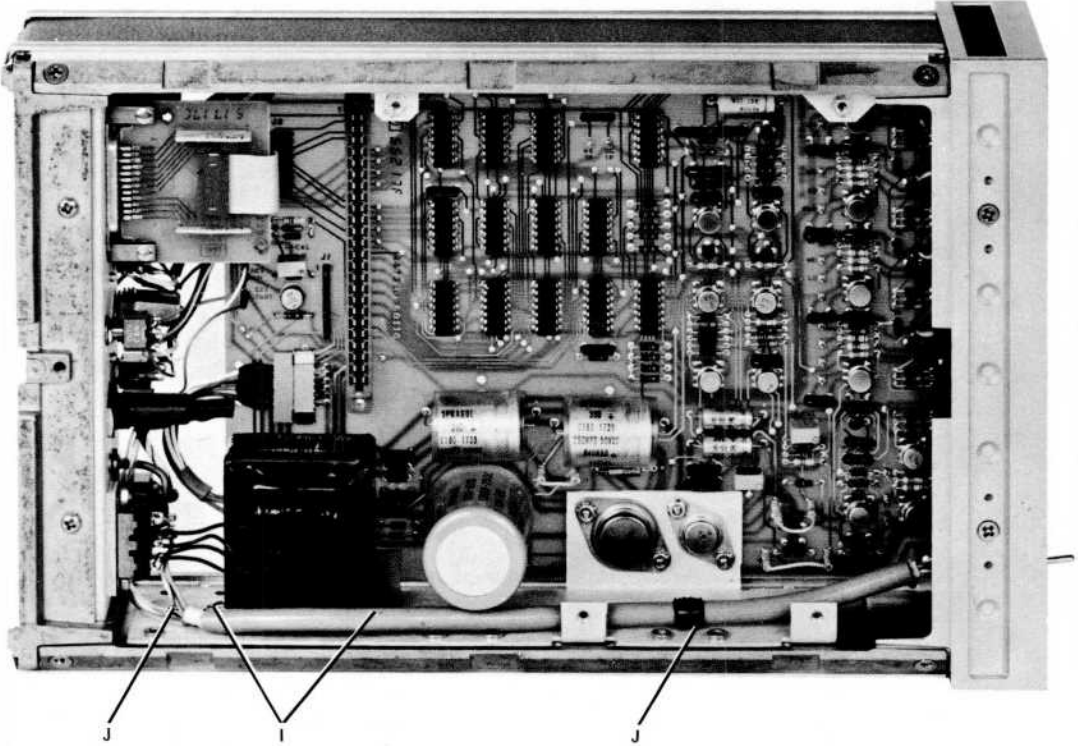


Figure 5-1. Disassembly (5 of 6)

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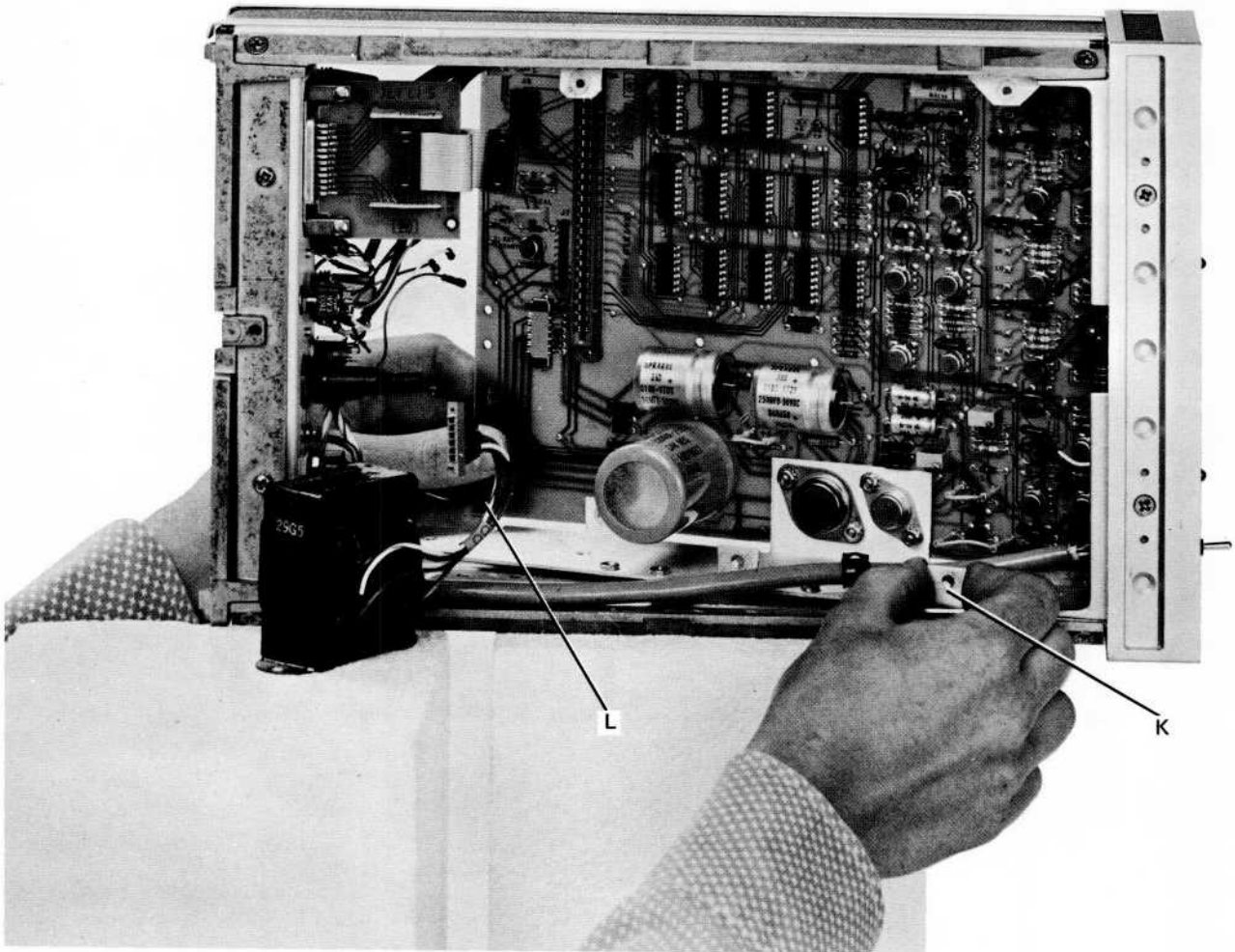


Figure 5-1. Disassembly (6 of 6)

Table 5-2. Program Commands

The Model 47310A responds to the following program characters:

Pace Rate Selection

A	—	One conversion only
B	—	200 Hz
C	—	100 Hz
D	—	50 Hz
E	—	20 Hz
F	—	10 Hz
G	—	5 Hz

Channel Selection

1	—	Chan 1
2	—	Chan 2
4	—	Chan 3
8	—	Chan 4

Control

H	—	Reset (all except rev. ch.)
I	—	Stop (pacer)
J	—	Start (pacer)
K	—	External Start Enable
L	—	SRQ Enable
M	—	SRQ Disable
N	—	Reverse Chan. on
O	—	Reverse Chan. off

Universal Bus Commands

Binary

Equiv.

20	—	Device Clear
24	—	Serial Poll Enable
25	—	Serial Poll Disable
63	—	Unlisten
95	—	Untalk

5-11. Sending an address of universal bus command* means that the bus controller (the desktop calculator) is programmed to:

- (1) Set the ATN line LO (assertive).
- (2) Apply to the bus data input and output (DIO) lines the desired ASCII address/command code.
- (3) Perform the bus handshake.
- (4) Set the ATN line HI (non-assertive).

5-12. Sending a control character* means that the bus controller is programmed to:

- (1) Send the 59313A LISTEN address as described above.
- (2) Apply to the bus DIO lines the desired ASCII control character code. See Table 5-2 for control characters.
- (3) Perform the bus handshake.

*Refer to the manual for the controller in use to determine how to do this.

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5-13. Performance Check.

5-14. Perform the minimum performance checks in order.

5-15. AC POWER CHECK.

Action	Result
a. Plug in the AC power cord.	
b. Connect a standard HP-IB cable between the controller and 59313A.	
c. Turn on the 59313A POWER switch.	The POWER lamp comes ON. The TALKER lamp stays OFF.

5-16. ADDRESSING CHECK.

Action	Result
a. (1) Send TALK Address.	TALKER lamp comes ON.
(2) Send LISTEN Address.	TALKER lamp goes OFF.
b. (1) Send TALK Address.	TALKER lamp comes ON.
(2) Send Un-talk Command.	TALKER lamp goes OFF.
c. (1) Send TALK Address.	TALKER lamp comes ON.
(2) Send all <i>other</i> Talk Addresses (pause between each).	TALKER lamp goes OFF at first "other" address and stays off at every other.
d. (1) Send TALK Address.	TALKER lamp comes ON.
(2) Send DEVICE CLEAR Command.	TALKER lamp goes OFF.
e. (1) Send TALK Address.	TALKER lamp comes ON.
(2) Set HP-IB IFC line (interface clear) momentarily LO (active).	TALKER lamp goes OFF.
f. (1) Send TALK Address.	TALKER lamp comes ON.
(2) Send all <i>other</i> LISTEN Addresses.	TALKER lamp comes on after all characters are sent and ATN line is HI.


5-17. REVERSE CHANNEL CHECK.

Action	Result
a. (1) Set the power supply to +5V ±0.1V; connect – to GND.	
(2) Connect Logic Probe supply leads to power supply.	
(3) Connect Logic Probe point to rear panel RVS CHAN jack (mini-phone plug connector).	Probe indicates OPEN circuit.
b. Send Control Character N (REV CHAN ON).	Probe indicates LO.
c. Send Control Character O (REV CHAN OFF).	Probe indicates OPEN circuit.
d. Send Control Character N .	Probe indicates LO.
e. Send Control Character H .	Probe stays LO.
f. (1) Send UN-listen Command ? .	
(2) <i>Without</i> first sending Listen Address, send Control Character O .	Probe stays LO.
g. Send Device Clear Command.	Probe indicates OPEN circuit.

5-18. A/D CONVERTER CHECK. This check tests whatever range the channel happens to be set to. If desired the range selection jumper can be moved to another position and this check repeated for each of the other 3 ranges. See Figure 2-2 for the range selection jumper positions.

a. Connect the variable power supply to one of the 4 channel inputs, and program the controller to do the following loop:

- (1) Send Control Characters **H** **8** **A** **J** (preceded by Listen Address).



Channel select character
for channel under test.
- (2) Send Talk Address.
- (3) Read and store 2 bytes of data from the HP-IB.
- (4) Process the 2 bytes of data and display the result. (See operating section for processing information.)
- (5) Start over again.

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- b. Vary the selected channel input voltage. The controller display should vary from 0 to +1023 and from 0 to -1024. The display should follow and be proportional to the input voltage over the entire range.
- c. Increase the input voltage to roughly twice that required to produce a display of +1023 (positive full scale). The display should stay at +1023.
- d. Repeat Step c for negative full scale (-1024).
- e. Remove the phone plug from the channel being tested. Set the rear panel CAL switch to -1. The controller display should be at some negative number between -80 and -1024.
- f. Change the CAL switch to 0. The display should change to some number between -40 and +40.
- g. (1) Connect the variable power supply to one of the channels not currently being tested.
(2) Vary the supply from about -15V to +15V while watching the controller display. The display should not vary as the supply changes.
- h. Repeat Step g for the other two channels not currently being tested.

5-19. LINEARITY CHECK.

- a. Program the controller with the same loop as used in the A to D Converter check.
- b. Connect the variable power supply to the channel to be tested.
- c. Connect the digital voltmeter across the power supply to monitor the voltage.
- d. Make and record a series of input voltage vs A to D output measurements using the following guidelines:
 - (1) Take at least 7 measurements spread out over the whole plus and minus range (e.g., -1000, -700, -200, 0, +300, +800, +1000).
 - (2) When taking a measurement, say at 800, adjust the variable voltage supply until the controller display is flipping back and forth between 800 and 801. Try to get equal occurrence of both numbers.
 - (3) At this point record the DVM reading of the input voltage to at least .02% of reading accuracy.
 - (4) Record the corresponding A to D output on the controller display as the average of the 2 numbers, e.g., $(800 + 801)/2 = 800.5$.
- e. Mathematically determine the best straight line through the data points as follows:
 - (1) Call the input voltage points $X_1, X_2, X_3, \dots, X_n$
 - (2) Call the A to D output points $Y_1, Y_2, Y_3, \dots, Y_n$
 X_1, Y_1 are a pair of measurements taken together.
 $n =$ number of pairs.

- (3) Using the X, Y data points, calculate A, B, C and D below.

$$A = Y_1 + Y_2 + Y_3 \dots + Y_n$$

$$B = X_1 + X_2 + X_3 \dots + X_n$$

$$C = (X_1 Y_1) + (X_2 Y_2) + (X_3 Y_3) \dots + (X_n Y_n)$$

$$D = (X_1)^2 + (X_2)^2 + (X_3)^2 \dots + (X_n)^2$$

- (4) Using the values for A, B, C, and D, calculate b and m below. N = number of pairs.

$$b = (AD - CB) / (ND - B^2)$$

$$m = (NC - AB) / (ND - B^2)$$

- (5) Substitute the values for b and m into the equation.

$$Y_c = mX + b$$

f. Take each of the input voltage points $X_1, X_2, X_3 \dots X_n$ and, one at a time, substitute them in place of X in this equation and calculate a value for Y_c .

g. The difference between any calculated value Y_c and the measured value of Y (the one that goes with the X used in the calculation) should not exceed ± 0.51 .

NOTE: If desired, the other input ranges and/or other input channels may be tested in the same way.

5-20. SERVICE REQUEST CHECK. In this test, "test the SRQ line" can be done either with a logic probe on pin 10 of the HP-IB connector or with a controller program check (see controller manual). (SRQ line LO = assertive.)

- a. (1) Remove the phone plug from channel 1 input jack.
- (2) Switch the CAL switch to -5.
- b. (1) Send Listen Address.
- (2) Send Control Characters **H** **A** **L** **J**. (Preceded by Listen Address.)
- (3) Test SRQ line for LO state.
- c. (1) Send Control Character **H**.
- (2) Test SRQ line for HI state.
- d. (1) Send Control Characters **H** **A** **L** **J**.
- (2) Test SRQ line for LO state.
- e. (1) Send Device Clear Command.
- (2) Test SRQ line for HI state.

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- f. (1) Send Control Characters **H** **A** **L** **M** **J** .
(2) Test SRQ line for HI state.
- g. (1) Send Control Characters **H** **I** **A** **L** **J** .
(2) Test SRQ line for LO state.
- h. (1) Send Serial Poll Enable Command.
(2) Send Talk Address.
(3) Test SRQ line for HI state.
- i. (1) Read 1 byte from the HP-IB.
(2) Check for byte value = 64.
- j. (1) Send UN-talk Command.
(2) Send Serial Poll Disable Command.
(3) Send Talk Address.
(4) Read 2 bytes from the HP-IB.
(5) Process the 2 bytes (see operating section for details).
(6) Check processed number for value between -400 and -1024.
- k. (1) Send Serial Poll Enable Command.
(2) Send Talk Address.
(3) Read 1 byte of data from HP-IB.
(4) Check byte for value = 0.
- l. (1) Send Untalk Command.
(2) Send Serial Poll Disable.
(3) Send Talk Address.
(4) Attempt to read a byte of data from the HP-IB.
(5) Program should hang up (no data available). (The controller may be able to check for lack of data availability without attempting the read and causing a hang up.)

5-21. PACER ACCURACY CHECK.

- a. (1) Connect a counter to the HP-IB SRQ line. (SRQ line is pin 10 on the HP-IB piggyback connector.)
- (2) Set the counter to the time interval mode.
- b. (1) Send control characters **H** **G** **L** **J** (preceded by Listen Address)


↑
Pace Select Character
- (2) Send Talk Address.
- (3)  Read two bytes from HP-IB.
Continue in loop.
- (4) Time interval on counter should be as in chart below.
- c. Substitute the next pace select character in the control character string and repeat the test.

Table 5-3. Pacer Accuracy Check

Pace Select Character	Pace Interval	±.05% Limits
G	200 ms	199.9 to 200.10
F	100 ms	99.95 to 100.05
E	50 ms	49.97 to 50.02
D	20 ms	19.99 to 20.01
C	10 ms	9.995 to 10.005
B	5 ms	4.997 to 5.002

NOTES:

1. The controller must be fast enough to read the two bytes in less time than the interval being tested.
2. A less accurate check of pace intervals can be made by programming the controller to take a large number of samples and timing, with a stopwatch or clock second hand, how long it takes.

$$\text{PACE INTERVAL} = \frac{\text{Number of Samples}}{\text{Time}}$$

5-22. EXTERNAL START CHECK.

- a. (1) Send Control Characters **H** **A** .
- (2) Send Talk Address.
- (3) Read 1 byte from HP-IB.
- (4) Display the byte.
- (5) Program hangs up at reading the byte.

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- b. (1) Ground the EXT STRT jack.
(2) Program still hangs.
- c. (1) Send Control Characters **H** **A** **K** .
(2) Send Talk Address.
(3) Read 1 byte from HP-IB.
(4) Display the byte on the controller.
(5) Program still hangs up at reading the byte.
- d. (1) Ground the rear panel EXT STRT jack.
(2) Some number is displayed.
- e. Repeat Steps c and d, except trigger external start by ungrounding (open circuit) the EXT STRT jack.

5-23. HP-IB verification program using the 9825A Calculator. Table 5-4 contains instructions for running a 9825A calculator program (available on cassette - HP Part No. 59300-10001) to check the 59313A for proper operation of the HP-IB I/O. This program is a shortened version of the minimum performance check (paragraph 5-7) and should be used accordingly.

5-24. ADJUSTMENTS.

5-25. Two of the channel inputs should have a phone plug inserted and two should not, and the instrument covers should be on. Turn on the power and warm up the instrument for at least 10 minutes. (Minimum performance checks with covers closed can be done during this time.) The temperature will be fully stabilized in about 2 hours.

5-26. Perform the adjustment as follows:

NOTE: Try to work quickly so internal cooling is minimized.

- a. Turn off the power by disconnecting the power cord.
- b. Remove the top cover.
- c. Remove the 4 screws holding the top circuit board to the brackets.
- d. By the transformer there is a place where the forefinger can reach under both the Top and Middle circuit boards. Pull up with the finger, thereby disengaging the connector.
- e. Insert the Top board edge connector (that normally faces the rear) into the socket in the bottom board so the Top and Middle boards (which are bolted together) stand on end.
- f. (1) Connect the DVM between the +15 TEST POINT and chassis ground.
(2) Adjust the +15 pot (R81 Bottom board) so the DVM reads $+15.000 \pm 2$ mV (14.998 to 15.002).
- g. (1) Connect the DVM between the -15 TEST POINT and chassis ground.
(2) The DVM should read between -14.5 and -15.5 (no adjustment).

- h. (1) Connect the DVM between the center pin on the rear panel CAL switch and chassis ground.
(2) Place the switch in its -5 position.
(3) Adjust the -5 pot (R54 Bottom board) so the DVM reads -5.000 ± 1 mV (-4.999 to -5.001).
- i. (1) Place the switch in its -1 position.
(2) Adjust -1 pot (R53 Bottom board) so the DVM reads -1.0000 ± 0.1 mV (-0.9999 to -1.0001).
- j. (1) Place the switch in its 0 position. The DVM should read 0 .0000 to $\pm 0 .00001$ (no adjustment).
- k. (1) Connect the DVM between the +5 TEST POINT and chassis ground.
(2) DVM reads 4.75 to 5.25 volts (no adjustment).
- l. Reassemble the 59313A.

5-27. TROUBLESHOOTING.

5-28. If the 59313A fails to pass any of the performance verification checks, try to determine whether the trouble is at the bus controller end of the line, or at the 59313A. A bus analyzer can monitor the transfer of Addresses, Commands, and Control Characters from the controller to the 59313A and the transfer of output from the 59313A to the controller. The controller (or its program) is defective if wrong codes are sent to the 59313A or if it ruins valid data from the 59313A. The 59313A is defective if it responds incorrectly to valid data from the controller or if it places incorrect data on the bus.

5-29. Since many of the 16 bus lines are shared, sometimes being driven by the controller, sometimes by the 59313A, it may be difficult to tell which end is at fault. In these cases it may be desirable to exercise the controller and/or the 59313A alone with the bus analyzer to determine the culprit.

5-30. If the 59313A is proven defective, the next step is to isolate the trouble to one of the 59313A circuit boards. Because of the large amount of interaction between boards this is most easily accomplished by trying known good boards (from the service kit) in place of the unknown ones until the unit works. Verify the +5-volt supply (4.75V to 5.25V) and then try the Top-Middle board assembly. If the problem is not cured, that leaves the bottom board as the most likely suspect.

5-31. Once the defective board is isolated, it can be replaced with the new one or an attempt to repair the old one can be made. On the bottom board, the analog signal circuitry is usually not too difficult to repair and most of the digital problems can be tracked down with the logic probe and bus controller manipulation. On the top and middle boards, which are all digital, some failures can be very easy to isolate using only the logic probe, while others can be extremely difficult, requiring a good scope and familiarity with the circuits.

Table 5-4. HP-IB Verification Program Using the 9825A Calculator

1. Figure A is the basic flowchart for the verification program.
2. Verification using the 9825A calculator.
 - a. Set up the 9825A Calculator with the 98213A General I/O-Extended I/O ROM or the 98214A Plotter-General I/O-Extended I/O ROM, 98034A HP-IB Calculator Interface (Address 7), and the 59313A for operation.
 - b. On the 59313A, select the HI input range on all four channels by moving jumpers on the bottom circuit board (refer to paragraph 2-20).
 Select address 00110 by moving jumpers on the underside of the top circuit board. This is the factory-set standard address (refer to paragraph 2-21).
 Set the ZERO and GAIN controls such that a 0-volt input produces a 0-output and a ±-volt input produces a ±1000-output (all four channels).
 Set the CAL switch to 0 volts and apply no external input while running the verification program.
 - c. Initialize the 59313A by turning the power off and on.
 - d. Insert the 59300 Series Verification Tape (HP Part No. 59300-10001) into the 9825A. Load and run file 0 (ldp0).
3. Program sequence of events and check points.
 File 0 on the tape contains the main program that accesses the individual programs for each of the HP-IB Programmable Modules. For example, in the main program (file 0) typing in "59313" causes file 13 to be loaded and run. File 13 contains the verification program (V.P.) for the 59313A Analog to Digital Converter. (See V.P. listing Figure B and sample 9825A printer output Figure C.) To continue the V.P. after each halt below, press the CONTINUE key on the 9825A.
 - a. The V.P. halts to verify the initial state of the 59313A:

CHECK POINT 1:	ON light	ON (remainder of the test)
	TALKER light	OFF
	CAL switch	0 volts
 - b. When the CONTINUE key on the 9825A is pressed, the V.P. (1) addresses the 59313A to listen (Handshake and Address Logics), (2) sends ASCII H11AJ (Reset, Channel Select, Pace Select, and Conversion Logics), (3) addresses the 59313A to talk, and (4) displays the 59313A output. The above sequence is then repeated for channels 2, 3, and 4. The display should show a zero for all four channels. The V.P. halts to verify:

CHECK POINT 2:	TALKER light	ON
	9825A display	Channel 4 A/D 0
 - c. Change the CAL switch to -1-volt. When the CONTINUE key is pressed, the sequence in b is repeated and the 9825A displays the 59313A output for the four channels. The V.P. halts to verify:

CHECK POINT 3:	TALKER light	ON
	9825A display	Channel 4 A/D -200
 - d. Change the CAL switch to -5 volts. When the CONTINUE key is pressed, the sequence in b is repeated and the 9825A displays the 59313A output for the four channels. The V.P. halts to verify:

CHECK POINT 4:	TALKER light	ON
	9825A display	Channel 4 A/D -10000
 - e. When the CONTINUE key is pressed, the V.P. (1) addresses the 59313A to listen, (2) sends ASCII H11BJ (pacer rate of 200 Hz), (3) addresses the 59313A to talk 25 times and (4) displays the 59313A output 25 times. The above sequence is then repeated for pacer rates of 100 50, 20, 10, and 5 Hz (ASCII H11CJ, H11DJ, H11EJ, H11FJ, H11GJ). The V.P. halts to verify:

CHECK POINT 5:	TALKER light	ON
	9825A display	Rate = 5 Hz; A/D #25 = -1000

Table 5-4. HP-IB Verification Program Using the 9825A Calculator (Cont'd)

- f. When the CONTINUE key is pressed, the V.P. (1) addresses the 59313A to listen, (2) sends ASCII H22LGJ (Reset, Serial Poll, Channel Select, Pace Select, and Conversion Logics), (3) and enters a loop where the SRQ line is continually monitored. When SRQ goes low (1) the status byte of the 59313A is examined, (2) the 59313A is addressed to talk, and (3) the 59313A output is displayed. The monitor loop is re-entered and the above process is repeated 25 times. The V.P. halts to verify:
- | | | |
|----------------|---------------|------------------------------|
| CHECK POINT 6: | TALKER light | ON |
| | 9825A display | Byte 64, Count 25, A/D -1000 |
- g. When the CONTINUE key is pressed, the Interface Clear command (cli) is sent. The V.P. halts to verify:
- | | | |
|----------------|--------------|-----|
| CHECK POINT 7: | TALKER light | OFF |
|----------------|--------------|-----|
- h. END OF TEST.

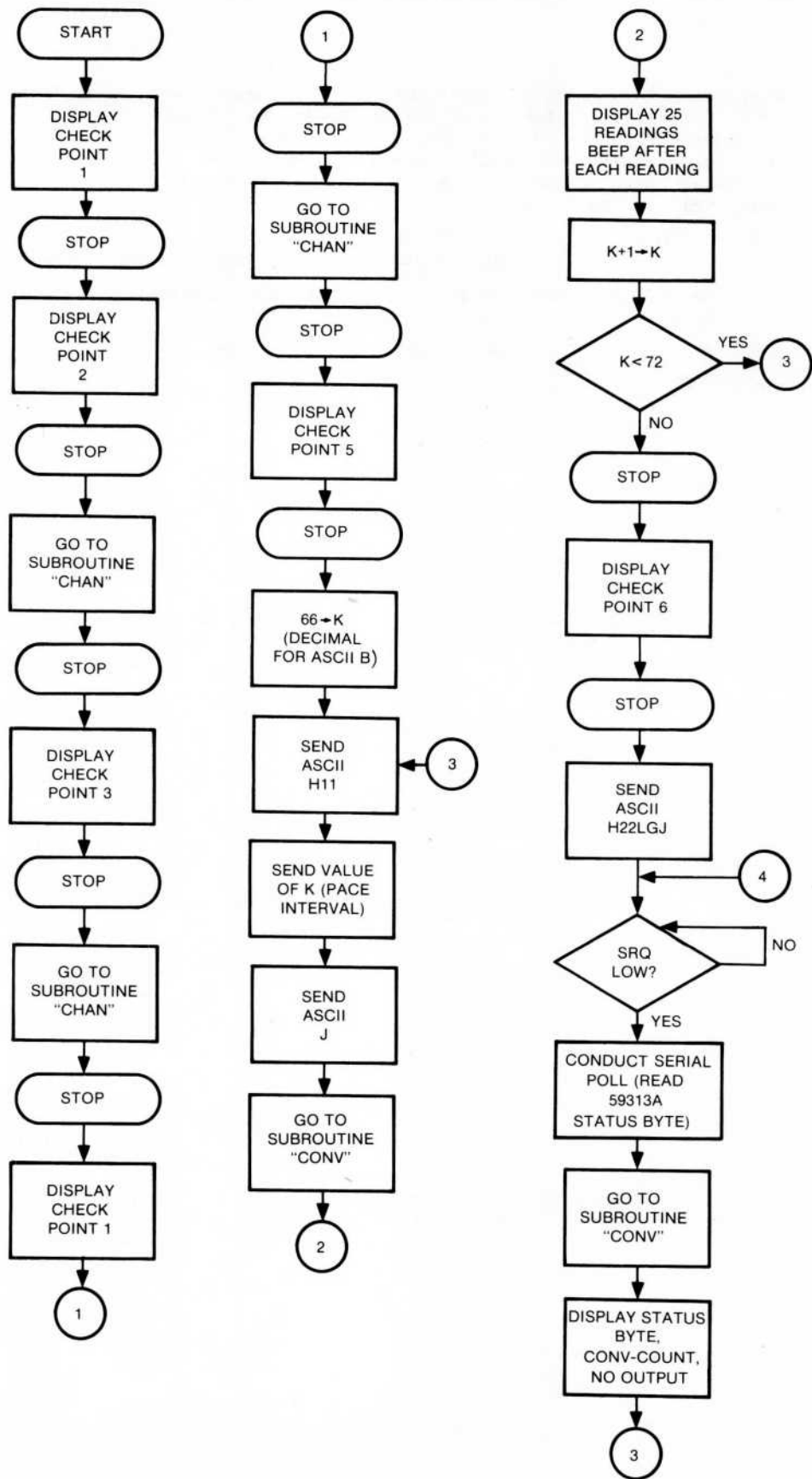


Figure A. 59313A Verification Program Flowchart

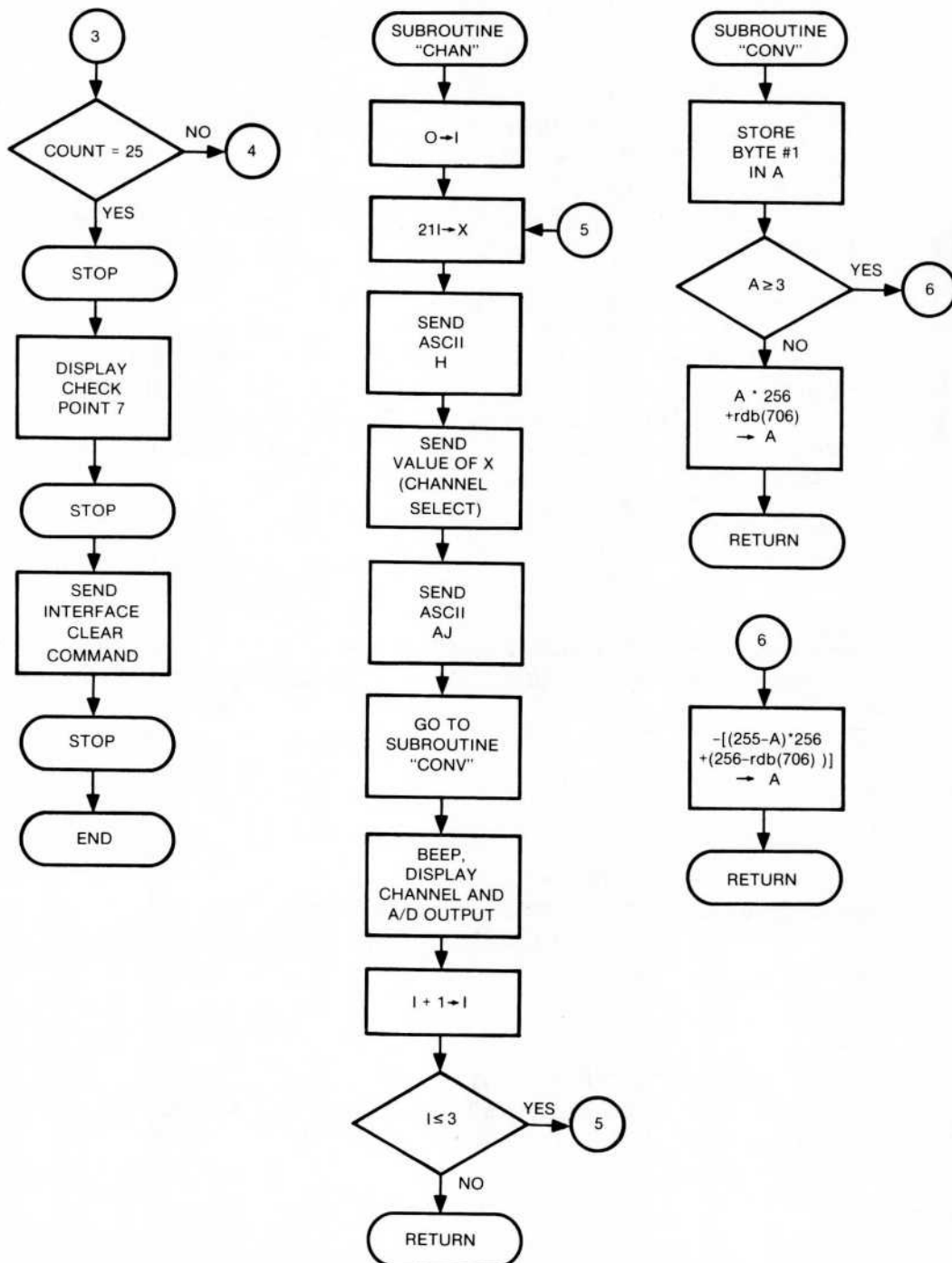


Figure A. 59313A Verification Program Flowchart (Cont'd)

Section V – Maintenance
Model 59313A

```
0: fxd 0
1: prt "59313","A/D Converter","Verification","Program";spc 2
2: prt "-----","CHECK POINT 1"
3: prt "Verify initial","setup:"
4: prt "*ON          on","*TALKER      off","*CAL swtch  0";spc 2
5: dsp "CHECK POINT 1"
6: stp
7: prt "-----","CHECK POINT 2"
8: prt "When CONTINUE","is pressed,"
9: prt "address 59313A","and send ASCII:"," H          (reset)"
10: prt " * (channel *)"," A (one conv)"," J          (start)"
11: prt "where * takes","the values 1-4","i.e. channels","1 thru 4.";spc 1
12: prt "Read each","channel of the","59313A, beep","and display"
13: prt "output for each","channel.,""Verify:"
14: prt "*TALKER      on","*dsp A/D      0";spc 2
15: dsp "CHECK POINT 2"
16: stp
17: gsb "chan"
18: stp
19: prt "-----","CHECK POINT 3"
20: prt "Change CAL to -1","and press","CONTINUE.";spc 1
21: prt "Verify:"
22: prt "*TALKER      on","*dsp A/D    -200";spc 2
23: dsp "CHECK POINT 3"
24: stp
25: gsb "chan"
26: stp
27: prt "-----","CHECK POINT 4"
28: prt "Change CAL to -5","and press","CONTINUE.";spc 1
29: prt "Verify:","*TALKER      on","*dsp A/D -1000";spc 2
30: dsp "CHECK POINT 4"
31: stp
32: gsb "chan"
33: stp
34: prt "-----","CHECK POINT 5"
35: prt "Pacer mode","check. Address","59313A and send:"
36: prt " H          (reset)"," 1 (channel 1)"," *          (rate *)"
```

Figure B. 59313A Verification Program Listing


```

37: prt " J      (start)", "where * takes", "the values", "B,C,D,E,F,G"
38: prt "for rates of", "200,100,50,20", "10, and 5 Hz."; spc 1
39: prt "When CONTINUE", "is pressed:"
40: prt "read 59313A", "beep and display", "25 conversions", "at each rate."
41: prt "Verify:"
42: prt "*TALKER      cn", "*dsp A/D -1000"; spc 2
43: dsp "CHECK POINT 5"
44: stp
45: 66→K
46: 400→L
47: fmt 2,z,3f.0
48: fmt 3,z,b
49: wrt 706.2, "H11"
50: wrt 706.3, K
51: wrt 706.2, "J"
52: 0→I
53: if 65<K and K<69; L/2→L
54: if K=69; (L-10)/2→L
55: if K>69; L/2→L
56: gsb "conv"
57: fxd 0
58: dsp "Rate=", L, "Hz;", "A/D #", I+1, "=", A
59: beep
60: I+1→I
61: if I<25; gto 56
62: wait 1000
63: K+1→K
64: if K<72; gto 49
65: stp
66: prt "-----", "CHECK POINT 6"
67: prt "When CONTINUE is", "pressed, send:"
68: prt " H      (reset)", " 2 (channel 2)", " L (SRQ enable)"
69: prt " C (5 Hz rate)", " J      (start)"; spc 1
70: prt "This enables", "SERVICE REQUEST."; spc 1
71: prt "The calculator", "should beep and", "the display"
72: prt "counter will", "count to 25."; spc 1
73: prt "The displayed", "status byte", "should = 64"; spc 1
74: prt "The displayed", "A/D conversion", "should = -1000"; spc 2
75: dsp "CHECK POINT 6"
76: stp
  
```

Section V - Maintenance
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```
77: 0→N
78: fmt 1,z,6f.0
79: wrt 706.1,"H22LGJ"
80: rds(7)→D
81: if bit(7,D);gto 83
82: gto 80
83: N+1→N
84: rds(706)→S
85: gsb "conv"
86: fxd 0
87: dsp "Byte",S,"Count",N," ,A/D",A
88: beep
89: if N=25;gto 91
90: gto 80
91: stp
92: prt "-----","CHECK POINT 7"
93: prt "Verify:","*TALKER      on";spc 1
94: prt "When CONTINUE is","pressed, the IFC","command is sent:"
95: prt "Verify:","*TALKER      off";spc 2
96: dsp "CHECK POINT 7"
97: stp
98: cli 7
99: dsp "CHECK POINT 7"
100: stp
101: gto 123
102: "conv":
103: rdb(706)→A
104: if A>3;gto 107
105: A*256+rdb(706)→A
106: ret
107: -((255-A)*256+(256-rdb(706)))→A
108: ret
109: "chan":
110: 0→I
111: fmt 1,z,2f.0
112: wrt 706.1,"H"
113: 2^I→X
114: wrt 706.1,X
115: wait 1000
116: wrt 706.1,"AJ"
117: gsb "conv"
118: beep
119: dsp "Channel=",I+1,"      A/D=",A
120: I+I→I
121: if I<=3;gto 112
122: ret
123: prt "END OF TEST";spc 4
124: rew
125: end
*3206
```

```

59313
A/D Converter
Verification
Program

-----
CHECK POINT 1
Verify initial
setup:
*DN          on
*TALKER      off
*CAL switch  0

-----
CHECK POINT 2
When CONTINUE
is pressed,
address 59313A
and send ASCII:
H      (reset)
*      (channel *)
A      (one conv)
J      (start)
where * takes
the values 1-4
i.e. channels
1 thru 4.

Read each
channel of the
59313A; beep
and display
output for each
channel.
Verify:
*TALKER      on
*dsp A/D    0

-----
CHECK POINT 3
Change CAL to -1
and press
CONTINUE.

Verify:
*TALKER      on
*dsp A/D    -200

-----
CHECK POINT 4
Change CAL to -5
and press
CONTINUE.

Verify:
*TALKER      on
*dsp A/D    -1000

-----
CHECK POINT 5
Pacer mode
check. Address
59313A and send:
H      (reset)
1      (channel 1)
*      (rate *)
J      (start)
where * takes
the values
B,C,D,E,F,G
for rates of
200,100,50,20,
10, and 5 Hz.

When CONTINUE
is pressed:
read 59313A,
beep and display
25 conversions
at each rate.
Verify:
*TALKER      on
*dsp A/D    -1000

-----
CHECK POINT 6
When CONTINUE is
pressed, send:
H      (reset)
2      (channel 2)
L      (SRQ enable)
G      (5 Hz rate)
J      (start)

-----
CHECK POINT 7
Verify:
*TALKER      on

When CONTINUE is
pressed, the IFC
command is sent:
Verify:
*TALKER      off

-----
END OF TEST

-----
This enables
SERVICE REQUEST.

The calculator
should beep and
the display
counter will
count to 25.

The displayed
status byte
should = 64

The displayed
A/D conversion
should = -1000

```

Figure C. 59313A Verification Program Sample Output

NOTES

SECTION VI REPLACEABLE PARTS

6-1. INTRODUCTION.

6-2. This section contains schematics, figures and information for identifying, locating and ordering replaceable parts.

6-3. Table 6-3 lists parts in order of the reference designations (circuit references) and provides the following information for each item.

- a. Description of the part (see Table 6-1 for abbreviations). Attaching parts, if any, follow the description.
- b. Typical manufacturer of the part using a five-digit code. See the code list of manufacturers in Table 6-2.
- c. Manufacturer's part number.
- d. Total quantity used in the instrument (Qty column).

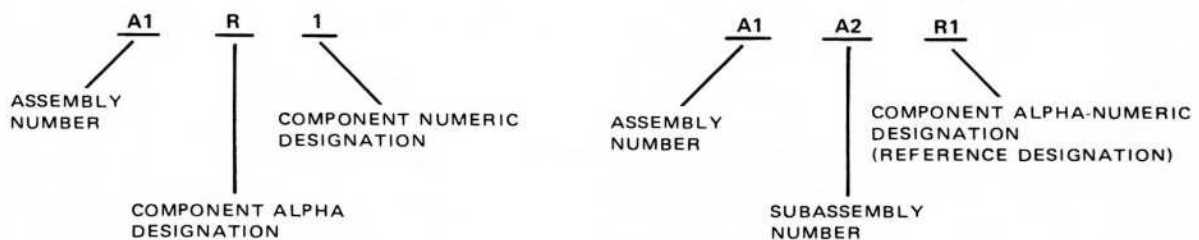
6-4. REFERENCE DESIGNATIONS.

6-5. Table 6-3 is based on an alpha-numerical method of listing the assemblies, subassemblies and circuit components. These items are defined as follows:

a. Each assembly and subassembly is assigned an "A" number (A1, A2, A3, etc). Assemblies and subassemblies that can be purchased have part numbers in the part number column; those that cannot be purchased have the word "Reference" in the column.

b. Components within the assembly and subassembly circuits are assigned circuit reference designators (C1 capacitor, R1 resistor, etc.). These parts are prefaced by the assembly number (A1C1, A2C2, A1R1, A2R2, etc.) to indicate the assembly on which the part is located.

6-6. Examples of the alpha-numeric numbering method used to identify assemblies, subassemblies and circuit components follow:



6-7. Partial reference designations are normally used on the equipment and illustrations. The partial reference designation consists of the component alpha designation and numeric designation. The complete reference designations are obtained by placing the proper assembly number (and subassembly number, when applicable) before the partial reference designations.

6-8. In this section, these assembly prefix numbers are usually shown with each reference designation, in the title of the figure or at the bottom of the illustration block following the notation "REF DESIG PREFIX." The complete reference designation should be used to easily locate a part and the description in the Parts List.

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Model 59313A

6-9. For example, to determine the value and the part number of resistor R6 in the A2 assembly (A2R6), locate the A2 group listing (the second group) in the parts list. Then refer to the R (resistor) designations in the group and find R6. The value and the part number are in the columns adjacent to the description.

6-10. ORDERING INFORMATION.

6-11. To order a replacement part, address order or inquiry to the local Hewlett-Packard Sales/Service Office (see list of addresses at the rear of this manual) and supply the HP part number of the item from Table 6-3.

6-12. To order a part not listed in the table, provide the following information:

- a. Model number of the instrument.
- b. Complete serial number of the instrument.
- c. Description of the part including function and location.

6-13. To order a part from a manufacturer other than Hewlett-Packard Company provide the complete part description and the manufacturer's part number from Table 6-3.

Table 6-1. List of Abbreviations

#	number	CYL	cylinder
"	inch(es)	DBL	double
A	assembly, amperes	DIP	dual in-line flat pack (for integrated circuit)
A/F	across flats (nut)	DIV	divider
A/R	as required	DO	package type, diode
ADJ	adjust, adjustable	ELECTRN	electron
AL	aluminum	ELEK	electronic
ASSY	assembly	EXT	external
AT	amperes — time delay	EXTR	external
BARR	barrier	F	female, film
BLK	block, black	FEM	female
BRS	brass	FIL	filament, fillister (screw head type)
C	cermet, capacitor, capacitance	FL	flat, flash, fluid, full
CALC	calculation, calculator	FLM	film
CC	carbon composition, cubic centimeters	FT	foot, feet gain X bandwidth product
CER	ceramic	HD	head, heavy-duty
CHAM	chamfer, chamfered	HEX	hexagonal
CHAN	channel	HLCL	helical
CLR	clear, clearance	HS	high speed, heat sealed, heat shrink
CM	centimeters	HYB	hybrid
CONT	contact		

Table 6-1. List of Abbreviations (Continued)

ID	inside diameter	REC	recess, recessed
IEC	International Electro-technical Commission	RECT	rectifier
IN	inch(es)	REINF	reinforced
INCL	including	RND	round
IND	indicator, inductance	SCR	screw, silicon-controlled rectifier (thyristor)
JEDEC	Joint Electron Device Engineering Councils	SEL	selector, selected
JU	jumper	SENS	sensitive
LG	long	SGL	single
LK	lock	SHLDR	shoulder
LKG	locking	SI	silicon
LKWR	lockwasher (LKWASH)	SKT	socket
L/S	liters per second	SLDR	solder
LV	low voltage	SOL	solenoid
MACH	machine	SPCL	special
MC	microcircuit	SST	stainless steel
MF	microfarad	STA	station
MINTR	miniature (MIN., MINAT.)	STD	standard
MO	metal oxide	STL	steel
MOSFET	metal oxide substrate field effect transistor	SUBMIN	subminiature
MS	millisecond	T-2	lamp bulb envelope shape (T), size in eighths of an inch (2 = 1/4-IN.), typical
MTG	mounting	TA	Tantalum (TANT)
MTLC	metallic	TC	temperature coefficient, time constant
MYL	Mylar	TGL	toggle
NPT	National Pipe Thread	THD	thread
NYL	Nylon (polyamide)	THK	thick
OBD	order by description	TO	package type, transistor
OD	outside diameter	TRMR	trimmer (TRIM.)
OPT	option (OPN)	UF	microfarad (MF)
PCB	printed circuit board	UNC	Unified National coarse (machine screw thread)
PD	power dissipation	UNF	Unified National fine (machine screw thread)
PF	Power factor, picofarad, peak flow, pipe female (pipe connection)	US	microsecond
PHL	phillips (cross slot screw head type)	VAR	variable
PLSTC	plastic	VOL	volume
PNEUM	pneumotach	W	white
POLYC	polycarbonate	WD	wide
POLYE	polyester	W/	with
PS	power supply	WVDC	working volts dc
PT	pint, part, point, pulse time	X	by (dimensional)
PVC	vinyl (polyvinyl chloride)	ZNR	Zener (breakdown diode)
PWR	power		

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Table 6-2. Code List of Manufacturers

MFR NO.	MANUFACTURER NAME	ADDRESS	ZIP CODE
00000	ANY SATISFACTORY SOURCE		
0007K	KABELMETAL		
00809	CROVEN LTD	ONTARIO CANADA	
00853	SANGAMO ELEC CO S CAROLINA DIV	PICKENS SC	29671
01121	ALLEN-BRADLEY CO	MILWAUKEE WI	53212
01295	TEXAS INSTR INC SEMICOND CMPNT DIV	DALLAS TX	75231
03888	KDI PYROFILM CORP	WHIPPANY NJ	07981
04713	MOTOROLA SEMICONDUCTOR PRODUCTS	PHOENIX AZ	85008
07263	FAIRCHILD SEMICONDUCTOR DIV	MOUNTAIN VIEW CA	94040
07707	USM CORP USM FASTENER DIV	SHELTON CT	06484
09023	CORNELL-DUBILIER ELEK DIV FED PAC	SANFORD NC	27330
09353	C AND K COMPONENTS INC	WATERTOWN MA	02172
16299	CORNING GL WK ELEK CMPNT DIV	RALEIGH NC	27604
19701	MEPCO/ELECTRA CORP	MINERAL WELLS TX	76067
19738	AVDEL CORP	TETERBORO NJ	07608
24226	GOWANDA ELECTRONICS CORP	GOWANDA NY	14070
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD PA	16701
27014	NATIONAL SEMICONDUCTOR CORP	SANTA CLARA CA	95051
27264	MOLEX PRODUCTS CO	DOWNERS GROVE IL	60515
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO CA	94304
28520	HEYMAN MFG CO	KENILWORTH NJ	07033
32293	INTERSIL INC	CUPERTINO CA	95014
32997	BOURNS INC TRIMPOT PROD DIV	RIVERSIDE CA	92507
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS MA	01247
71400	BUSSMAN MFG DIV OF MCGRAW-EDISON CO	ST LOUIS MO	63017
71785	TRW ELEK COMPONENTS CINCH DIV	ELK GROVE VILLAGE IL	60007
72136	ELECTRO MOTIVE CORP SUB IEC	WILLIMANTIC CT	06226
73138	BECKMAN INSTRUMENTS INC HELIPOT DIV	FULLERTON CA	92634
73743	FISCHER SPECIAL MFG CO	CINCINNATI OH	45206
75915	LITTELFUSE INC	DES PLAINES IL	60016
78189	ILLINOIS TOOL WORKS INC SHAKEPROOF	ELGIN IL	60126
82389	SWITCHCRAFT INC	CHICAGO IL	60630
83330	SMITH HERMAN H INC	BROCKLYN NY	11207
84411	TRW CAPACITOR DIV	OGALLALA NE	69153
91662	ELCO CORP	WILLOW GROVE PA	19090
95987	WECKESSER CO INC	CHICAGO IL	60641

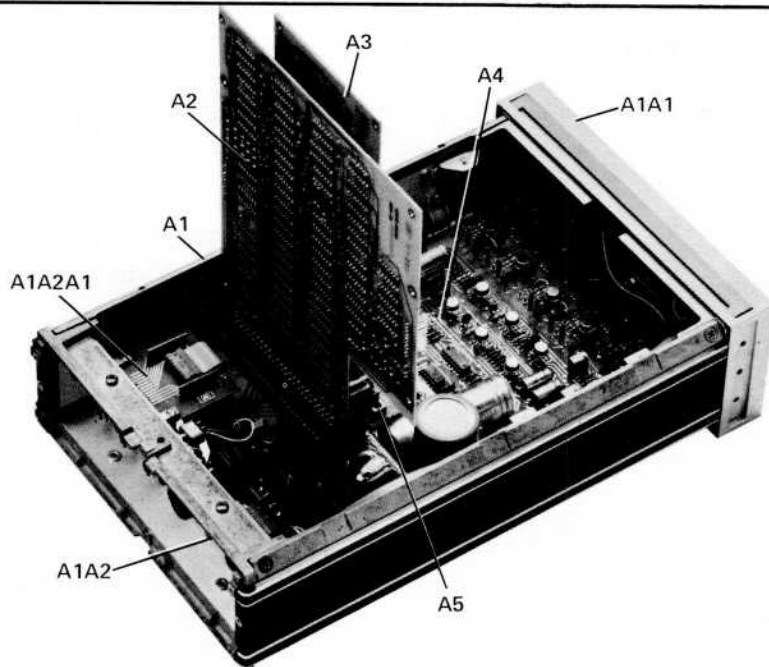


Figure 6-1. Assembly Locations

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
LIST OF ASSEMBLIES (FIGURE 6-1)					
A1	NSN	1	CASE ASSEMBLY	28480	NSN
A1A1	REFERENCE 2360-0181	1 4	FRONT PANEL ASSEMBLY SCREW-MACH 6-32 .25-IN-LG 82 DEG	28480 28480	REFERENCE 2360-0181
A1A2	47310-60030 2360-0115	1 10	REAR PANEL ASSEMBLY SCREW-MACH 6-32 .312-IN-LG PAN-HD-POZI	28480 28480	47310-60030 2360-0115
A1A2A1	47310-60150	1	INTERFACE P.C. ASSEMBLY	28480	47310-60150
A2	47310-60120 2360-0113	1 4	P.C. ASSEMBLY, TOP SCREW-MACH 6-32 .25-IN-LG PAN-HD-POZI	28480 28480	47310-60120 2360-0113
A3	47310-60130 0380-0526	1 2	P.C. ASSEMBLY, MIDDLE STANDOFF-RND .875LG 6-32THD .2500 BRS	28480 83330	47310-60130 8785
A4	47310-60110 1400-0017 2360-0115	1 1	P.C. ASSEMBLY, BOTTOM CLAMP-CA .375-IN-WD NYL SCREW-MACH 6-32 .312-IN-LG PAN-HD-POZI	28480 28520 28480	47310-60110 3305 2360-0115
A5	47310-60140	1	P.C. ASSEMBLY, INTERCONNECTION	28480	47310-60140
A6	47310-63498		ACCESSORIES	28480	47310-63498

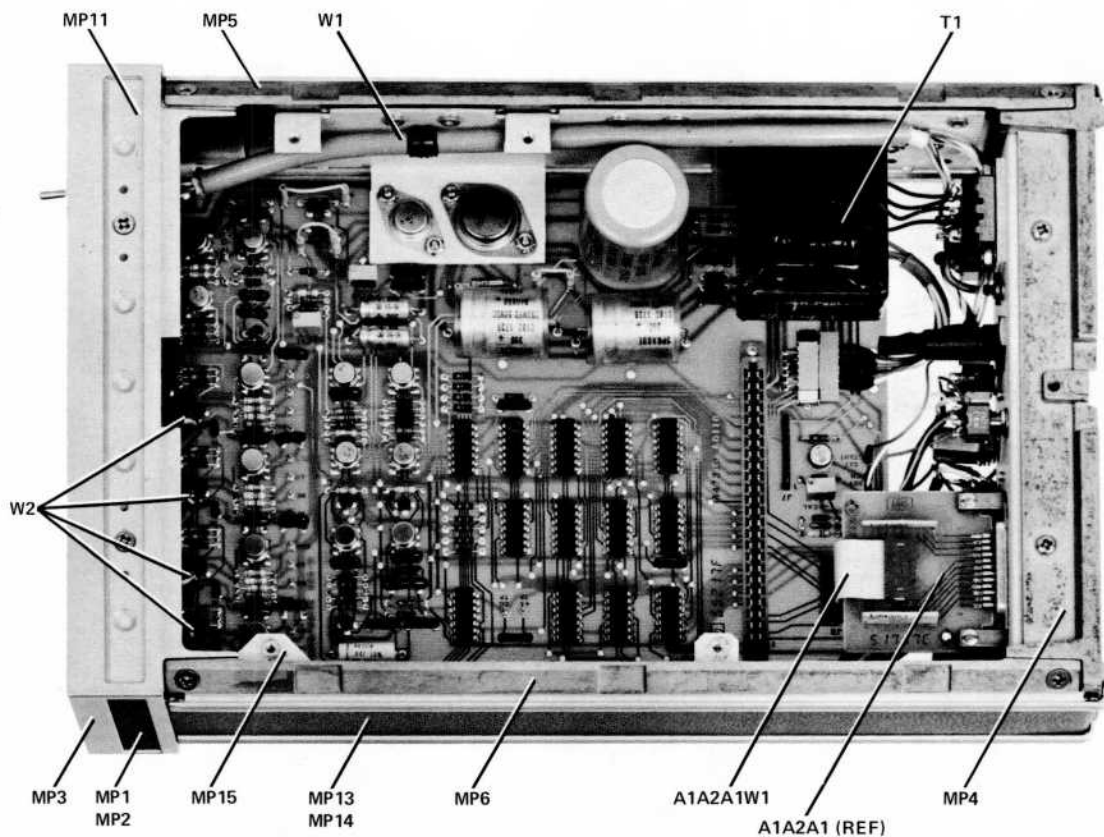


Figure 6-2. Component Locations, Case Assembly A1

Section VI — Replaceable Parts
Model 59313A

Table 6-3. Replaceable Parts (Continued)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A1	NSN	1	CASE ASSEMBLY (FIGURE 6-2)	28480	NSN
A1MP1	5001-0438	2	TRIM, SIDE FRONT	28480	5001-0438
A1MP2	5001-0438		TRIM, SIDE FRONT	28480	5001-0438
A1MP3	5020-8813	1	FRAME, FRONT	28480	5020-8813
A1MP4	5020-8814	1	FRAME, REAR	28480	5020-8814
A1MP5	5020-8830	2	SIDE STRUT	28480	5020-8830
	2510-0192	8	SCREW-MACH 8-32 .25-IN-LG 100 DEG	28480	2510-0192
A1MP6	5020-8830		SIDE STRUT	28480	5020-8830
	2510-0192		SCREW-MACH 8-32 .25-IN-LG 100 DEG	28480	2510-0192
A1MP7	5040-7201	4	FOOT(STANDARD)	28480	5040-7201
A1MP8	5040-7201		FOOT(STANDARD)	28480	5040-7201
A1MP9	5040-7201		FOOT(STANDARD)	28480	5040-7201
A1MP10	5040-7201		FOOT(STANDARD)	28480	5040-7201
A1MP11	5040-7203	1	TRIM:TOP 1/2	28480	5040-7203
A1MP12	5001-1418	1	COVER, BOTTOM	28480	5001-1418
A1MP13	5060-9850	2	COVER, SIDE (STANDARD)	28480	5060-9850
A1MP14	5060-9850		COVER, SIDE (STANDARD)	28480	5060-9850
A1MP15	47310-00040	1	Mounting BRACKET, RIGHT	28480	47310-00040
	1400-0059	2	CLAMP-CA .5-IN-WD NYL	95987	7/16-FN
	2360-0115	11	SCREW-MACH 6-32 .312-IN-LG PAN-HD-POZI	28480	2360-0115
A1MP16	5060-9829	0	TOP COVER	28480	5060-9829
A1T1	47310-60101	1	UL TRANSFORMER ASSEMBLY	28480	47310-60101
	2360-0113	2	SCREW-MACH 6-32 .25-IN-LG PAN-HD-POZI	28480	2360-0113
A1W1	47310-60060	1	CABLE, POWER	28480	47310-60060
A1W2	47310-60070	4	CABLE, INPUT	28480	47310-60070
A1A1	REFERENCE	1	FRONT PANEL ASSEMBLY (FIGURE 6-3)	28480	REFERENCE
A1A1MP1	47310-60012	1	FRONT PANEL, GRAY	28480	47310-60012
A1A1MP2	1490-0968	8	BUSHING-PNL .14-ID .3-LG 1/4-32-THD	28480	1490-0968
	2950-0072	10	NUT-HEX-DBL-CHAM 1/4-32-THD .062-THK	82389	P-1975
A1A1MP3	1490-0968		BUSHING-PNL .14-ID .3-LG 1/4-32-THD	28480	1490-0968
	2950-0072		NUT-HEX-DBL-CHAM 1/4-32-THD .062-THK	82389	P-1975
A1A1MP4	1490-0968		BUSHING-PNL .14-ID .3-LG 1/4-32-THD	28480	1490-0968
	2950-0072		NUT-HEX-DBL-CHAM 1/4-32-THD .062-THK	82389	P-1975
A1A1MP5	1490-0968		BUSHING-PNL .14-ID .3-LG 1/4-32-THD	28480	1490-0968
	2950-0072		NUT-HEX-DBL-CHAM 1/4-32-THD .062-THK	82389	P-1975
A1A1MP6	1490-0968		BUSHING-PNL .14-ID .3-LG 1/4-32-THD	28480	1490-0968
	2950-0072		NUT-HEX-DBL-CHAM 1/4-32-THD .062-THK	82389	P-1975
A1A1MP7	1490-0968		BUSHING-PNL .14-ID .3-LG 1/4-32-THD	28480	1490-0968
	2950-0072		NUT-HEX-DBL-CHAM 1/4-32-THD .062-THK	82389	P-1975
A1A1MP8	1490-0968		BUSHING-PNL .14-ID .3-LG 1/4-32-THD	28480	1490-0968
	2950-0072		NUT-HEX-DBL-CHAM 1/4-32-THD .062-THK	82389	P-1975
A1A1MP9	1490-0968		BUSHING-PNL .14-ID .3-LG 1/4-32-THD	28480	1490-0968
	2950-0072		NUT-HEX-DBL-CHAM 1/4-32-THD .062-THK	82389	P-1975
A1A1MP10	1400-0560	2	CLIP SET-LED MTG FOR PNL MTG HP LED	28480	1400-0560
A1A1MP11	1400-0560		CLIP SET-LED MTG FOR PNL MTG HP LED	28480	1400-0560
A1A1S1	3101-1508	1	SWITCH-TGL SUBMIN DPDT NS 2A 250VAC	09353	U318-HI
	2190-0027	7	WASHER-LK INTL T NO.-1/4 .256-IN-ID	78189	1914-00
	3050-0273	4	WASHER-FL MTLC NO.-1/4 .261-IN-ID	28480	3050-0273
A1A2	47310-60030	1	REAR PANEL ASSEMBLY (FIGURE 6-4)	28480	47310-60030
A1A2C35	0160-0677	1	CAPACITOR-FXD .01UF +-20% 250WVAC CER	56289	36C218A7
A1A2F1	2110-0235	1	FUSE .2A 250V SLU-BLD 1.25X.25 UL IEC	75915	313.200S
A1A2J1	1251-1779	4	CONNECTOR-TEL JACK 3-CKTS .25-SHK-DIA	82389	13B
	2190-0027		WASHER-LK INTL T NO.-1/4 .256-IN-ID	78189	1914-00
	2950-0043	4	NUT-HEX-DBL-CHAM 3/8-32-THD .094-THK	73743	2X 28200
A1A2J2	2190-0082	4	WASHER-LK INTL T NO.-3/8 .384-IN-ID	78189	1220-00
	1251-1779		CONNECTOR-TEL JACK 3-CKTS .25-SHK-DIA	82389	13B
	2190-0027		WASHER-LK INTL T NO.-1/4 .256-IN-ID	78189	1914-00
	2950-0043		NUT-HEX-DBL-CHAM 3/8-32-THD .094-THK	73743	2X 28200
	2190-0082		WASHER-LK INTL T NO.-3/8 .384-IN-ID	78189	1220-00
A1A2J3	1251-1779		CONNECTOR-TEL JACK 3-CKTS .25-SHK-DIA	82389	13B
	2190-0027		WASHER-LK INTL T NO.-1/4 .256-IN-ID	78189	1914-00
	2950-0043		NUT-HEX-DBL-CHAM 3/8-32-THD .094-THK	73743	2X 28200
	2190-0082		WASHER-LK INTL T NO.-3/8 .384-IN-ID	78189	1220-00
A1A2J4	1251-1779		CONNECTOR-TEL JACK 3-CKTS .25-SHK-DIA	82389	13B
	2190-0027		WASHER-LK INTL T NO.-1/4 .256-IN-ID	78189	1914-00
	2950-0043		NUT-HEX-DBL-CHAM 3/8-32-THD .094-THK	73743	2X 28200
	2190-0082		WASHER-LK INTL T NO.-3/8 .384-IN-ID	78189	1220-00
A1A2J5	1251-2230	2	CONNECTOR-TEL JACK 2-CKTS .141-SHK-DIA	82389	142A
	2190-0027		WASHER-LK INTL T NO.-1/4 .256-IN-ID	78189	1914-00
	2950-0072		NUT-HEX-DBL-CHAM 1/4-32-THD .062-THK	82389	P-1975
	3050-0273		WASHER-FL MTLC NO.-1/4 .261-IN-ID	28480	3050-0273
A1A2J6	1251-2230		CONNECTOR-TEL JACK 2-CKTS .141-SHK-DIA	82389	142A
	2190-0027		WASHER-LK INTL T NO.-1/4 .256-IN-ID	78189	1914-00

Section VI — Replaceable Parts
Model 59313A

Table 6-3. Replaceable Parts (Continued)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A1A2J7	2950-0072 3050-0273 1251-2357 2200-0105	1	NUT-HEX-DBL-CHAM 1/4-32-THD .062-THK WASHER-FL MTLCL NO.-1/4 .261-IN-ID CONNECTOR, AC POWER HP-9 MALE FLANGE SCREW-MACH 4-40 .312-IN-LG PAN-HD-POZI	82389 28480 92389 28480	P-1975 3050-0273 EAC-301 2200-0105
A1A2MP1 A1A2MP2	47310-00030 7122-0097 0361-0490	1 1 2	REAR PANEL SER PLT *SERIAL NO; HEWLETT PACKARD- RIVET, BLIND, DOME-HD .094" DIA	28480 91345 07707	47310-00030 080 AD-32A55
A1A2S1 A1A2S2	3101-1911 0361-0009 3101-0963 2190-0273 3050-0273	1 2 1 1	SWITCH, SLIDE RIVET, SEMITUBULAR OVAL HD 0.188" LG SWITCH-TGL SUBMIN SPDT NS 5A 115VAC WASHER, FLAT WASHER-FL MTLCL NO.-1/4 .261-IN-ID	82389 00000 09353 00000 28480	11A-1477 080 7103-SY 080 3050-0273
A1A2XF1	2110-0481 2190-0037	1 1	FUSEHOLDER-EXTR POST 20A 300V UL/IEC WASHER-LK INTL T NO.-1/2 .512-IN-ID	75915 78189	345003 1224-08
A1A2A1	47310-60150	1	INTERFACE P.C. ASSEMBLY (FIGURE 6-5)	28480	47310-60150
A1A2A1H1 A1A2A1H2	0380-0644 1530-1098	1 1	STANDOFF-HEX 6/32" FASTENER:0.136" DIA 6-32 THREAD	00000 00000	080 080
A1A2A1J1 A1A2A1J2	1251-3283 1200-0473	1 2	CONNECTOR; 24-CONT; FEM; MICRORIBBON SOCKET-IC 16-CONT DIP-SLDR	28480 78303	1251-3283 C931602
A1A2A1R1 A1A2A1R2	1810-0136 1810-0136	2	NETWORK-RES 10-PIN-SIP .1-PIN-SPCG NETWORK-RES 10-PIN-SIP .1-PIN-SPCG	56289 56289	216C 216C
A1A2A1U1	47310-00150 0361-0434 2190-0034	1 2 2	P.C. BOARD, BLANK RIVET, BLIND PL THRU, DOME-HD .125"DIA WASHER-LK HLCL NO.-10 .194-IN-ID	28480 19738 28480	47310-00150 1125-0412 2190-0034
A1A2A1W1	47310-60040	1	CABLE ASSEMBLY, INTERFACE BOARD	28480	47310-60040
A2	47310-60120	1	TOP P.C. ASSEMBLY (FIGURE 6-6)	28480	47310-60120
A2C1 A2C2 A2C3 A2C4 A2C5 A2C6	0180-2062 0160-3097 0160-2709 0160-3097 0160-3097	1 9 1	CAPACITOR-FXD 120UF+-20% 10VDC TA CAPACITOR-FXD .47UF +80-20% 50WVDC CER CAPACITOR-FXD 160PF +-1% 500WVDC MICA CAPACITOR-FXD .47UF +80-20% 50WVDC CER CAPACITOR-FXD .47UF +80-20% 50WVDC CER	56289 56289 72136 56289 56289	1500127X0010R2 5C54C2-CML R0M15F161F55 5C54C2-CML 5C54C2-CML
A2C7 A2C8	0160-3097 0160-3097	1 1	CAPACITOR-FXD .47UF +80-20% 50WVDC CER CAPACITOR-FXD .47UF +80-20% 50WVDC CER	56289 56289	5C54C2-CML 5C54C2-CML
A2CR1 A2CR2 A2CR3	1901-0025 1901-0025 1901-0025	3	DIODE-GEN PRP 100V 200MA DO-7 DIODE-GEN PRP 100V 200MA DO-7 DIODE-GEN PRP 100V 200MA DO-7	07263 07263 07263	FD-2389 FD-2389 FD-2389
A2J1	1251-2025 2340-0006 2200-0147 1251-3964	3 10 6 2	CONNECTOR-PC EDGE 24-CONT/ROW 2-ROWS NUT-HEX-DBL-CHAM 4-40-THD .094-THK SCREW-MACH 4-40 .5-IN-LG PAN-HD-POZI CONNECTOR 3-PIN M POST TYPE	71785 28480 28480 27264	252-24-30-340 2340-0006 2200-0147 22-11-2041
A2J4 A2J5	1251-3958 1251-3958	7	CONNECTOR 10-PIN M POST TYPE	27264	22-10-2101
A2L1	9100-2259	1	COIL-FXD MOLDED RF CHOKE 1.5UH 10%	24226	10/151
A2Q1 A2Q2	1853-0020 1853-0020	2	TRANSISTOR PNP SI PD=300MW FT=150MHZ TRANSISTOR PNP SI PD=300MW FT=150MHZ	01295 01295	SKA1123 SKA1123
A2R1 A2R2 A2R3 A2R4 A2R5	0683-1035 0757-0429 0757-0429 0757-0415 0757-0415	16 3	RESISTOR 10K 5% .25W FC TC=-400/+700 RESISTOR 1.82K 1% .125W F TC=0+-100 RESISTOR 1.82K 1% .125W F TC=0+-100 RESISTOR 475 1% .125W F TC=0+-100 RESISTOR 475 1% .125W F TC=0+-100	01121 24546 24546 24546 24546	CB1035 C4-1/8-T0-1821-F C4-1/8-T0-1821-F C4-1/8-T0-475R-F C4-1/8-T0-475R-F
A2R6 A2R7 A2R8 A2R9 A2R10	0757-0415 0683-1035 0683-1035 0683-1035 0683-1035	16	RESISTOR 475 1% .125W F TC=0+-100 RESISTOR 10K 5% .25W FC TC=-400/+700 RESISTOR 10K 5% .25W FC TC=-400/+700 RESISTOR 10K 5% .25W FC TC=-400/+700 RESISTOR 10K 5% .25W FC TC=-400/+700	24546 01121 01121 01121 01121	C4-1/8-T0-475R-F CB1035 CB1035 CB1035 CB1035
A2R11 A2R12 A2R13 A2R14 A2R15	0757-0415 0757-0415 0683-2715 0757-0429 0757-0415	16	RESISTOR 475 1% .125W F TC=0+-100 RESISTOR 475 1% .125W F TC=0+-100 RESISTOR 270 5% .25W FC TC=-400/+600 RESISTOR 1.82K 1% .125W F TC=0+-100 RESISTOR 475 1% .125W F TC=0+-100	24546 24546 01121 24546 24546	C4-1/8-T0-475R-F C4-1/8-T0-475R-F CB2715 C4-1/8-T0-1821-F C4-1/8-T0-475R-F
A2U1 A2U2 A2U3 A2U4	1820-0600 1820-0600 1820-0600 47310-00120 0360-1730	5 1 1 65	IC-DIGITAL DM74L90N TTL L DECD IC-DIGITAL DM74L90N TTL L DECD IC-DIGITAL DM74L90N TTL L DECD P.C. BOARD, BLANK TERMINAL-STUD SPCL-STDF PRESS-MTG	27014 27014 27014 28480 00779	DM74L90N DM74L90N DM74L90N 47310-00120 P75-31131-1
A2U5 A2U6 A2U7 A2U8 A2U9	1820-1442 1820-1442 1820-0600 1820-0587 1820-0584	2 2 5 9	IC-DIGITAL SN74LS290N TTL LS DECD IC-DIGITAL SN74LS290N TTL LS DECD IC-DIGITAL DM74L90N TTL L DECD IC-DIGITAL DM74L10N TTL L TPL 3 NAND IC-DIGITAL DM74L02N TTL L QUAD 2 NDR	01295 01295 27014 27014 27014	SN74LS290N SN74LS290N DM74L90N DM74L10N DM74L02N

See introduction to this section for ordering information

Section VI — Replaceable Parts
Model 59313A

Table 6-3. Replaceable Parts (Continued)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A2U10	1820-0596	11	IC-DIGITAL DM74L74N TTL L DUAL	27014	DM74L74N
A2U11	1820-0596		IC-DIGITAL DM74L74N TTL L DUAL	27014	DM74L74N
A2U12	1820-1425	2	IC-DIGITAL SN74LS132N TTL LS QUAD 2 NAND	01295	SN74LS132N
A2U13	1820-0583	11	IC-DIGITAL DM74L00N TTL L QUAD 2 NAND	27014	DM74L00N
A2U14	1820-0627	1	IC-DIGITAL 93L010C TTL L 4 BCD-TO-DEC	07263	93L010C
A2U15	1820-0596		IC-DIGITAL DM74L74N TTL L DUAL	27014	DM74L74N
A2U16	1820-0583		IC-DIGITAL DM74L00N TTL L QUAD 2 NAND	27014	DM74L00N
A2U17	1820-0054	2	IC-DIGITAL SN7400N TTL QUAD 2 NAND	01295	SN7400N
A2U18	1820-0596		IC-DIGITAL DM74L74N TTL L DUAL	27014	DM74L74N
A2U19	1820-0600		IC-DIGITAL DM74L90N TTL L DECD	27014	DM74L90N
A2U20	1820-0658	1	IC-DIGITAL 93L120C TTL L 8 8-TO-1-LINE	07263	93L120C
A2U21	1820-0595	5	IC-DIGITAL DM74L73N TTL L DUAL J-K	27014	DM74L73N
A2U22	1820-0586	1	IC-DIGITAL DM74L04N TTL L HEX 1	27014	DM74L04N
A2U23	1820-0584		IC-DIGITAL DM74L02N TTL L QUAD 2 NOR	27014	DM74L02N
A2U24	1820-0588	3	IC-DIGITAL DM74L20N TTL L DUAL 4 NAND	27014	DM74L20N
A2U25	1820-0583		IC-DIGITAL DM74L00N TTL L QUAD 2 NAND	27014	DM74L00N
A2U26	1820-0595		IC-DIGITAL DM74L73N TTL L DUAL J-K	27014	DM74L73N
A2U27	1820-0583		IC-DIGITAL DM74L00N TTL L QUAD 2 NAND	27014	DM74L00N
A2U28	1820-0584		IC-DIGITAL DM74L02N TTL L QUAD 2 NOR	27014	DM74L02N
A2U29	1820-1425		IC-DIGITAL SN74LS132N TTL LS QUAD 2 NAND	01295	SN74LS132N
A2U30	1820-0596		IC-DIGITAL DM74L74N TTL L DUAL	27014	DM74L74N
A2U31	1820-0583		IC-DIGITAL DM74L00N TTL L QUAD 2 NAND	27014	DM74L00N
A2U32	1820-0584		IC-DIGITAL DM74L02N TTL L QUAD 2 NOR	27014	DM74L02N
A2U33	1820-0587		IC-DIGITAL DM74L10N TTL L TPL 3 NAND	27014	DM74L10N
A2U34	1820-0584		IC-DIGITAL DM74L02N TTL L QUAD 2 NOR	27014	DM74L02N
A2U35	1820-0584		IC-DIGITAL DM74L02N TTL L QUAD 2 NOR	27014	DM74L02N
A2U36	1820-0588		IC-DIGITAL DM74L20N TTL L DUAL 4 NAND	27014	DM74L20N
A2U37	1820-0587		IC-DIGITAL DM74L10N TTL L TPL 3 NAND	27014	DM74L10N
A2U38	1820-0583		IC-DIGITAL DM74L00N TTL L QUAD 2 NAND	27014	DM74L00N
A2U39	1820-0596		IC-DIGITAL DM74L74N TTL L DUAL	27014	DM74L74N
A2U40	1820-0621	4	IC-DIGITAL SN7438N TTL QUAD 2 NAND	01295	SN7438N
A2Y1	0410-0436	1	CRYSTAL:QUARTZ 10 MHZ	00809	08D
	78205-63060	9	JUMPERS	28480	78205-63060
A3	47310-60130	1	MIDDLE P.C. ASSEMBLY (FIGURE 6-7)	28480	47310-60130
A3C1	0160-3097		CAPACITOR-FXD .47UF +80-20% 50WVDC CER	56289	5C54C2-CML
A3C2	0160-3097		CAPACITOR-FXD .47UF +80-20% 50WVDC CER	56289	5C54C2-CML
A3C3	0160-3097		CAPACITOR-FXD .47UF +80-20% 50WVDC CER	56289	5C54C2-CML
A3C4	0160-3097		CAPACITOR-FXD .47UF +80-20% 50WVDC CER	56289	5C54C2-CML
A3J2	1251-3958		CONNECTOR 10-PIN M POST TYPE	27264	22-10-2101
A3R1	0683-5625	12	RESISTOR 5.6K 5% .25W FC TC=-400/+700	01121	CB5625
A3R2	0683-5625		RESISTOR 5.6K 5% .25W FC TC=-400/+700	01121	CB5625
A3R3	0683-5625		RESISTOR 5.6K 5% .25W FC TC=-400/+700	01121	CB5625
A3R4	0683-5625		RESISTOR 5.6K 5% .25W FC TC=-400/+700	01121	CB5625
A3U1	1820-0595		IC-DIGITAL DM74L73N TTL L DUAL J-K	27014	DM74L73N
A3U2	1820-0596		IC-DIGITAL DM74L74N TTL L DUAL	27014	DM74L74N
A3U3	1820-0583		IC-DIGITAL DM74L00N TTL L QUAD 2 NAND	27014	DM74L00N
A3U4	1820-0595		IC-DIGITAL DM74L73N TTL L DUAL J-K	27014	DM74L73N
A3U5	1820-0584		IC-DIGITAL DM74L02N TTL L QUAD 2 NOR	27014	DM74L02N
A3U6	1820-0595		IC-DIGITAL DM74L73N TTL L DUAL J-K	27014	DM74L73N
A3U7	1820-0586		IC-DIGITAL DM74L20N TTL L DUAL 4 NAND	27014	DM74L20N
A3U8	1820-0583		IC-DIGITAL DM74L00N TTL L QUAD 2 NAND	27014	DM74L00N
A3U9	1820-0876	3	IC-DIGITAL SN74L75N TTL L D-TYPE	01295	SN74L75N
A3U10	1820-0778	3	IC-DIGITAL 93L160C TTL L BIN SYNCHRO	07263	93L160C
A3U11	1820-0587		IC-DIGITAL DM74L10N TTL L TPL 3 NAND	27014	DM74L10N
A3U12	1820-0054		IC-DIGITAL SN7400N TTL QUAD 2 NAND	01295	SN7400N
A3U13	1820-0621		IC-DIGITAL SN7438N TTL QUAD 2 NAND	01295	SN7438N
A3U14	1820-0710	2	IC-DIGITAL 93L220C TTL L QUAD 2	07263	93L220C
A3U15	1820-0876		IC-DIGITAL SN74L75N TTL L D-TYPE	01295	SN74L75N
A3U16	1820-0778		IC-DIGITAL 93L160C TTL L BIN SYNCHRO	07263	93L160C
A3U17	1820-0584		IC-DIGITAL DM74L02N TTL L QUAD 2 NOR	27014	DM74L02N
A3U18	1820-0596		IC-DIGITAL DM74L74N TTL L DUAL	27014	DM74L74N
A3U19	1820-0621		IC-DIGITAL SN7438N TTL QUAD 2 NAND	01295	SN7438N
A3U20	1820-0710		IC-DIGITAL 93L220C TTL L QUAD 2	07263	93L220C
A3U21	1820-0876		IC-DIGITAL SN74L75N TTL L D-TYPE	01295	SN74L75N
A3U22	1820-0778		IC-DIGITAL 93L160C TTL L BIN SYNCHRO	07263	93L160C
A3U23	NSN		NOT USED	28480	NSN
A3U24	47310-00130	1	P.C. BOARD, BLANK	28480	47310-00130

Table 6-3. Replaceable Parts (Continued)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A4	47310-60110	1	BOTTOM P.C. ASSEMBLY (FIGURE 6-9)	28480	47310-60110
A4C1	0150-0121	10	CAPACITOR-FXD .1UF +80-20% 50WVDC CER	56289	5C50B1-CML
A4C2	0150-0121		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	56289	5C50B1-CML
A4C3	0150-0121		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	56289	5C50B1-CML
A4C4	0150-0134	2	CAPACITOR-FXD 220PF +-5% 300WVDC MICA	72136	RDM15F221J3C
A4C5	0150-0134		CAPACITOR-FXD 220PF +-5% 300WVDC MICA	72136	RDM15F221J3C
A4C6	0160-2208	4	CAPACITOR-FXD 330PF +-5% 300WVDC MICA	72136	RDM15F331J3C
A4C7	0160-3465	1	CAPACITOR-FXD .047UF +-10% 50WVDC POLYLC	84411	4630W4739R5W2
A4C8	0160-2204	7	CAPACITOR-FXD 100PF+-5% 300WVDC MICA	09023	RDM15F101J3C
A4C9	0150-0121		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	56289	5C50B1-CML
A4C10	0150-0121		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	56289	5C50B1-CML
A4C11	0160-2218	1	CAPACITOR-FXD 1000PF +-5% 300WVDC MICA	28480	0160-2218
A4C12	0140-0197	1	CAPACITOR-FXD 180PF +-5% 300WVDC MICA	72136	QM15F181J0300WV1CR
A4C13	0180-2026	1	C:FXD ELECT 3200 UF +100-10% 25VDCW	00853	505
A4C14	0150-0121		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	56289	5C50B1-CML
A4C15	0180-2060	1	CAPACITOR-FXD 40UF+-20% 10VDC TA	56289	1500406X0010B2
A4C16	0150-0121		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	56289	5C50B1-CML
A4C17	0150-0121		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	56289	5C50B1-CML
A4C18	0180-1739	2	CAPACITOR-FXD 250UF+75-10% 50VDC AL	56289	390257G050HE4
A4C19	0180-1739		CAPACITOR-FXD 250UF+75-10% 50VDC AL	56289	390257G050HE4
A4C20	0180-0183	2	CAPACITOR-FXD 10UF+75-10% 50VDC AL	56289	3001066050C82
A4C21	0180-0183		CAPACITOR-FXD 10UF+75-10% 50VDC AL	56289	3001066050C82
A4C22	0150-0121		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	56289	5C50B1-CML
A4C23	0150-0121		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	56289	5C50B1-CML
A4C24	0160-0776	2	CAPACITOR-FXD 1500PF +-20% 1000WVDC CER	56289	C023B102F152MS25-CDH
A4C25	0160-0776		CAPACITOR-FXD 1500PF +-20% 1000WVDC CER	56289	C023B102F152MS25-CDH
A4C26	0160-2208		CAPACITOR-FXD 330PF +-5% 300WVDC MICA	72136	RDM15F331J3C
A4C27	0160-2208		CAPACITOR-FXD 330PF +-5% 300WVDC MICA	72136	RDM15F331J3C
A4C28	0160-2208		CAPACITOR-FXD 330PF +-5% 300WVDC MICA	72136	RDM15F331J3C
A4C29	0160-2204		CAPACITOR-FXD 100PF+-5% 300WVDC MICA	09023	RDM15F101J3C
A4C30	0160-2204		CAPACITOR-FXD 100PF+-5% 300WVDC MICA	09023	RDM15F101J3C
A4C31	0160-2204		CAPACITOR-FXD 100PF+-5% 300WVDC MICA	09023	RDM15F101J3C
A4C32	0160-2204		CAPACITOR-FXD 100PF+-5% 300WVDC MICA	09023	RDM15F101J3C
A4C33	0160-2204		CAPACITOR-FXD 100PF+-5% 300WVDC MICA	09023	RDM15F101J3C
A4C34	0160-2204		CAPACITOR-FXD 100PF+-5% 300WVDC MICA	09023	RDM15F101J3C
A4C35	0160-2198	1	CAPACITOR-FXD 20PF +-5% 300WVDC MICA	72136	RDM15C200J3C
A4CR1	1901-0053	6	DIODE-GEN PRP 30V 150MA DO-7	07263	FD3444
A4CR2	1901-0053		DIODE-GEN PRP 30V 150MA DO-7	07263	FD3444
A4CR3	1901-0053		DIODE-GEN PRP 30V 150MA DO-7	07263	FD3444
A4CR4	1901-0053		DIODE-GEN PRP 30V 150MA DO-7	07263	FD3444
A4CR5	1902-0685	1	DIODE-ZNR 9V 2% DO-7 PD=.5W TC=+.001%	04713	SZ 12169
A4CR6	1901-0053		DIODE-GEN PRP 30V 150MA DO-7	07263	FD3444
A4CR7	1901-0053		DIODE-GEN PRP 30V 150MA DO-7	07263	FD3444
A4CR8	1901-0028	5	DIODE-PRW RECT 400V 750MA DO-29	04713	SR1358-9
A4CR9	1901-0028		DIODE-PRW RECT 400V 750MA DO-29	04713	SR1358-9
A4CR10	1901-0363	1	DIODE-MULT FULL WAVE BRIDGE RECTIFIER	04713	SDA 10185-3
A4CR11	1901-0028		DIODE-PRW RECT 400V 750MA DO-29	04713	SR1358-9
A4CR12	1901-0028		DIODE-PRW RECT 400V 750MA DO-29	04713	SR1358-9
A4CR13	1901-0028		DIODE-PRW RECT 400V 750MA DO-29	04713	SR1358-9
A4J1	1251-2025		CONNECTOR-PC EDGE 24-CONT/ROW 2-ROWS	71785	252-24-30-340
	2200-0147		SCREW-MACH 4-40 .5-IN-LG PAN-HD-POZI	28480	2200-0147
	2340-0006		NUT-HEX-DBL-CHAM 4-40-THD .094-THK	28480	2340-0006
A4J2	1251-3958		CONNECTOR 10-PIN M POST TYPE	27264	22-10-2101
A4J3	1251-3958		CONNECTOR 10-PIN M POST TYPE	27264	22-10-2101
A4J4	1251-3958		CONNECTOR 10-PIN M POST TYPE	27264	22-10-2101
A4J5	1251-3964		CONNECTOR 3-PIN M POST TYPE	27264	22-11-2041
A4J6	1251-0664	1	CONNECTOR 6-PIN H RECTANGULAR	91662	00-8129-006-610-001
A4J7	1251-3958		CONNECTOR 10-PIN M POST TYPE	27264	22-10-2101
A4J8	1200-0473		SOCKET-IC 16-CONT DIP-SLDR	78303	C931602
A4MP2	47310-00050	1	HEAT SINK BRACKET	28480	47310-00050
	2200-0107	4	SCREW-MACH 4-40 .375-IN-LG PAN-HD-POZI	00000	0BD
	2340-0006		NUT-HEX-DBL-CHAM 4-40-THD .094-THK	00000	0BD
	2360-0115		SCREW-MACH 6-32 .312-IN-LG PAN-HD-POZI	00000	0BD
A4MP3	47310-00060	1	POT ALIGNMENT BRACKET	28480	47310-00060
A4Q1	1855-0406	8	TRANSISTOR J-FET P-CHAN D-MODE SI	32293	IT110
A4Q2	1855-0406		TRANSISTOR J-FET P-CHAN D-MODE SI	32293	IT110
A4Q3	1855-0406		TRANSISTOR J-FET P-CHAN D-MODE SI	32293	IT110
A4Q4	1855-0406		TRANSISTOR J-FET P-CHAN D-MODE SI	32293	IT110
A4Q5	1855-0406		TRANSISTOR J-FET P-CHAN D-MODE SI	32293	IT110
A4Q6	1855-0406		TRANSISTOR J-FET P-CHAN D-MODE SI	32293	IT110
A4Q7	1855-0406		TRANSISTOR J-FET P-CHAN D-MODE SI	32293	IT110
A4Q8	1855-0406		TRANSISTOR J-FET P-CHAN D-MODE SI	32293	IT110
A4Q9	1854-0263	1	TRANSISTOR NPN 2N3019 SI TO-5 PD=800MW	04713	2N3019
A4R1	0698-6977	9	RESISTOR 30K .1% .125W F TC=0+-25	24546	NE55
A4R2	0698-6336	4	RESISTOR 6.8K 1% .125W F TC=0+-25	24546	NE55
A4R3	0698-6624	5	RESISTOR 2K .1% .125W F TC=0+-25	24546	NE55
A4R4	0698-8191	7	RESISTOR 12.5K .1% .125W F TC=0+-25	19701	MF4C1/8-T9-1252-8
A4R5	0683-1035		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	C81035

See introduction to this section for ordering information

Section VI — Replaceable Parts
Model 59313A

Table 6-3. Replaceable Parts (Continued)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A4R6	2100-3161	8	RESISTOR-TRMR 20K 10% C SIDE-ADJ 17-TURN	32997	3006P-1-203
A4R7	0698-6977		RESISTOR 30K .1% .125W F TC=0+-25	24546	NE55
A4R8	0698-6620	4	RESISTOR 150K .1% .125W F TC=0+-25	03888	PME555
A4R9	2100-3161		RESISTOR-TRMR 20K 10% C SIDE-ADJ 17-TURN	32997	3006P-1-203
A4R10	0698-6977		RESISTOR 30K .1% .125W F TC=0+-25	24546	NE55
A4R11	0698-6336		RESISTOR 6.8K 1% .125W F TC=0+-25	24546	NE55
A4R12	0698-6624		RESISTOR 2K .1% .125W F TC=0+-25	24546	NE55
A4R13	0698-8191		RESISTOR 12.5K .1% .125W F TC=0+-25	19701	MF4C1/8-T9-1252-B
A4R14	0683-1035		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A4R15	2100-3161		RESISTOR-TRMR 20K 10% C SIDE-ADJ 17-TURN	32997	3006P-1-203
A4R16	0698-6977		RESISTOR 30K .1% .125W F TC=0+-25	24546	NE55
A4R17	0698-6620		RESISTOR 150K .1% .125W F TC=0+-25	03888	PME555
A4R18	2100-3161		RESISTOR-TRMR 20K 10% C SIDE-ADJ 17-TURN	32997	3006P-1-203
A4R19	0698-6977		RESISTOR 30K .1% .125W F TC=0+-25	24546	NE55
A4R20	0698-6336		RESISTOR 6.8K 1% .125W F TC=0+-25	24546	NE55
A4R21	0698-6624		RESISTOR 2K .1% .125W F TC=0+-25	24546	NE55
A4R22	0698-8191		RESISTOR 12.5K .1% .125W F TC=0+-25	19701	MF4C1/8-T9-1252-B
A4R23	0683-1035		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A4R24	2100-3161		RESISTOR-TRMR 20K 10% C SIDE-ADJ 17-TURN	32997	3006P-1-203
A4R25	0698-6977		RESISTOR 30K .1% .125W F TC=0+-25	24546	NE55
A4R26	0698-6620		RESISTOR 150K .1% .125W F TC=0+-25	03888	PME555
A4R27	2100-3161		RESISTOR-TRMR 20K 10% C SIDE-ADJ 17-TURN	32997	3006P-1-203
A4R28	0698-6977		RESISTOR 30K .1% .125W F TC=0+-25	24546	NE55
A4R29	0698-6336		RESISTOR 6.8K 1% .125W F TC=0+-25	24546	NE55
A4R30	0698-6624		RESISTOR 2K .1% .125W F TC=0+-25	24546	NE55
A4R31	0698-8191		RESISTOR 12.5K .1% .125W F TC=0+-25	19701	MF4C1/8-T9-1252-B
A4R32	0683-1035		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A4R33	2100-3161		RESISTOR-TRMR 20K 10% C SIDE-ADJ 17-TURN	32997	3006P-1-203
A4R34	0698-6977		RESISTOR 30K .1% .125W F TC=0+-25	24546	NE55
A4R35	0698-6620		RESISTOR 150K .1% .125W F TC=0+-25	03888	PME555
A4R36	2100-3161		RESISTOR-TRMR 20K 10% C SIDE-ADJ 17-TURN	32997	3006P-1-203
A4R37	0698-3442	1	RESISTOR 237 1% .125W F TC=0+-100	16299	C4-1/8-T0-237R-F
A4R38	0698-7847	1	RESISTOR 1.111K .1% .125W F TC=0+-25	19701	MF4C1/8-T9-1111R-B
A4R39	0698-7634	1	RESISTOR 42.2K 1% .125W F TC=0+-25	19701	MF4C1/8-T9-4222-F
A4R40	0757-0199	1	RESISTOR 21.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2152-F
A4R41	0698-5556	1	RESISTOR 3.3K 1% .125W F TC=0+-25	24546	NE55
A4R42	0698-6977		RESISTOR 30K .1% .125W F TC=0+-25	24546	NE55
A4R43	0757-0273	1	RESISTOR 3.01K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3011-F
A4R44	0698-8191		RESISTOR 12.5K .1% .125W F TC=0+-25	19701	MF4C1/8-T9-1252-B
A4R45	0698-8191		RESISTOR 12.5K .1% .125W F TC=0+-25	19701	MF4C1/8-T9-1252-B
A4R46	0757-0290	2	RESISTOR 6.19K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-6191-F
A4R47	0683-1035		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A4R48	0683-1035		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A4R49	0683-1035		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A4R50	0683-1035		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A4R51	0683-1035		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A4R52	0698-6624		RESISTOR 2K .1% .125W F TC=0+-25	24546	NE55
A4R53	2100-3083	1	RESISTOR-TRMR 500 10% C TOP-ADJ 20-TURNS	73138	66WR500
A4R54	2100-3534	1	RESISTOR, VAR 100 OHM	28480	2100-3534
A4R55	0683-5615	2	RESISTOR 560 5% .25W FC TC=-400/+600	01121	CB5615
A4R56	0698-6362	1	RESISTOR 1K .1% .125W F TC=0+-25	24546	NE55
A4R57	0698-6361	1	RESISTOR 6K .1% .125W F TC=0+-25	24546	NE55
A4R58	0698-6630	1	RESISTOR 20K .1% .125W F TC=0+-25	24546	NE55
A4R59	0698-6627	1	RESISTOR 25K .1% .125W F TC=0+-25	24546	NE55
A4R60	0683-1035		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A4R61	0757-0289	1	RESISTOR 13.3K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-1332-F
A4R62	0757-0280	2	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A4R63	0698-3154	1	RESISTOR 4.22K 1% .125W F TC=0+-100	16299	C4-1/8-T0-4221-F
A4R64	0698-4121	1	RESISTOR 11.3K 1% .125W F TC=0+-100	16299	C4-1/8-T0-1132-F
A4R65	0698-8191		RESISTOR 12.5K .1% .125W F TC=0+-25	19701	MF4C1/8-T9-1252-B
A4R66	0683-5625		RESISTOR 5.6K 5% .25W FC TC=-400/+700	01121	CB5625
A4R67	0698-6353	2	RESISTOR 50K .1% .125W F TC=0+-25	03888	PME555
A4R68	0698-6353		RESISTOR 50K .1% .125W F TC=0+-25	03888	PME555
A4R69	0683-5625		RESISTOR 5.6K 5% .25W FC TC=-400/+700	01121	CB5625
A4R70	0683-5625		RESISTOR 5.6K 5% .25W FC TC=-400/+700	01121	CB5625
A4R71	0683-5625		RESISTOR 5.6K 5% .25W FC TC=-400/+700	01121	CB5625
A4R72	0683-5625		RESISTOR 5.6K 5% .25W FC TC=-400/+700	01121	CB5625
A4R73	0698-4009	1	RESISTOR 50K 1% .125W F TC=0+-100	16299	C4-1/8-T0-5002-F
A4R74	0683-5625		RESISTOR 5.6K 5% .25W FC TC=-400/+700	01121	CB5625
A4R75	0683-1035		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A4R76	0757-0284	1	RESISTOR 150 1% .125W F TC=0+-100	24546	C4-1/8-T0-151-F
A4R77	0683-5625		RESISTOR 5.6K 5% .25W FC TC=-400/+700	01121	CB5625
A4R78	0683-5625		RESISTOR 5.6K 5% .25W FC TC=-400/+700	01121	CB5625
A4R79	0683-5615		RESISTOR 560 5% .25W FC TC=-400/+600	01121	CB5615
A4R80	0757-0280		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F

Table 6-3. Replaceable Parts (Continued)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A4R81	2100-3097	1	RESISTOR-TRMR 100K 10% C TOP-ADJ	73138	66WR100K
A4R82	0683-0515	2	RESISTOR 5.1 5% .25W FC TC=-400/+500	01121	CB51G5
A4R83	0683-0515		RESISTOR 5.1 5% .25W FC TC=-400/+500	01121	CB51G5
A4R84	0698-4409	2	RESISTOR 127 1% .125W F TC=0+-100	16299	C4-1/8-T0-127R-F
A4R85	0757-0290		RESISTOR 6.19K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-6191-F
A4R86	0683-3315	1	RESISTOR 330 5% .25W FC TC=-400/+600	01121	CB3315
A4R87	0698-4409		RESISTOR 127 1% .125W F TC=0+-100	16299	C4-1/8-T0-127R-F
A4R88	0757-0389	1	RESISTOR 33.2 1% .125W F TC=0+-100	24546	C4-1/8-T0-33R2-F
A4U1	1820-1056	2	IC-DIGITAL SN74132N TTL QUAD 2 NAND	01295	SN74132N
A4U2	1820-0583		IC-DIGITAL DM74L00N TTL L QUAD 2 NAND	27014	DM74L00N
A4U3	1820-0587		IC-DIGITAL DM74L10N TTL L TPL 3 NAND	27014	DM74L10N
A4U4	1820-0514	1	IC-DIGITAL SN7426N TTL QUAD 2 NAND	01295	SN7426N
A4U5	1820-0059	4	IC LM 201A OP AMP	27014	LM201AH
A4U6	1820-1056		IC-DIGITAL SN74132N TTL QUAD 2 NAND	01295	SN74132N
A4U7	1820-0596		IC-DIGITAL DM74L74N TTL L DUAL	27014	DM74L74N
A4U8	1820-0621		IC-DIGITAL SN7438N TTL QUAD 2 NAND	01295	SN7438N
A4U9	1820-0596		IC-DIGITAL DM74L74N TTL L DUAL	27014	DM74L74N
A4U10	1820-0026	1	IC LM 311 COMPARATOR	27014	LM311H
A4U11	1820-0478	1	IC LM 308 OP AMP	27014	LM308H
A4U12	1820-0059		IC LM 201A OP AMP	27014	LM201AH
A4U13	1820-0584		IC-DIGITAL DM74L02N TTL L QUAD 2 NOR	27014	DM74L02N
A4U14	1820-0583		IC-DIGITAL DM74L00N TTL L QUAD 2 NAND	27014	DM74L00N
A4U15	1820-0583		IC-DIGITAL DM74L00N TTL L QUAD 2 NAND	27014	DM74L00N
A4U16	1820-0596		IC-DIGITAL DM74L74N TTL L DUAL	27014	DM74L74N
A4U18	1820-0043	7	IC LM 307 OP AMP	27014	LM307H
A4U19	1820-0043		IC LM 307 OP AMP	27014	LM307H
A4U20	1820-0059		IC LM 201A OP AMP	27014	LM201AH
A4U21	1820-0043		IC LM 307 OP AMP	27014	LM307H
A4U22	1820-0043		IC LM 307 OP AMP	27014	LM307H
A4U23	1820-0059		IC LM 201A OP AMP	27014	LM201AH
A4U24	1820-0043		IC LM 307 OP AMP	27014	LM307H
A4U25	1820-0430	1	IC LM 309 V RGLTR	27014	LM309K
A4U26	1820-0140	1	IC MC 1468 V RGLTR	04713	MC1468K
A4U27	1820-0043		IC LM 307 OP AMP	27014	LM307H
A4U28	1820-0043		IC LM 307 OP AMP	27014	LM307H
A4U29	47310-00110	1	P.C. BOARD, BLANK	28480	47310-00110
	0360-1730		TERMINAL-STUD SPCL-STDF PRESS-MTG	00779	P75-31131-1
	47310-90110	3	SCHEMATICS SHEETS	28480	47310-90110
A4W1	78205-63060		JUMPER	28480	78205-63060
A4W2	78205-63060		JUMPER	28480	78205-63060
A4W3	78205-63060		JUMPER	28480	78205-63060
A4W4	78205-63060		JUMPER	28480	78205-63060
A4W5	78205-63060		JUMPER	28480	78205-63060
A4W6	78205-63060		JUMPER	28480	78205-63060
A4W7	78205-63060		JUMPER	28480	78205-63060
A4W8	78205-63060		JUMPER	28480	78205-63060
A5	47310-60140	1	INTERCONNECT P.C. ASSEMBLY (FIGURE 6-8)	28480	47310-60140
A5J1	1251-2025		CONNECTOR-PC EDGE 24-CONT/ROW 2-ROWS	71785	252-24-30-340
	2200-0147		SCREW-MACH 4-40 .5-IN-LG PAN-HD-POZI	28480	2200-0147
	2340-0006		NUT-HEX-DBL-CHAM 4-40-THD .094-THK	28480	2340-0006
A5MP1	1251-1115	1	PL26 KEY-PRINTED CIRCUIT CONN	71785	456-07-35-003
A5U1	47310-00140	1	P.C. BOARD, BLANK	28480	47310-00140
A6	47310-63498	1	ACCESSORIES FOR 47310A	28480	47310-63498
	8710-0875	1	SCREWDRIVER	00000	080
	47310-91998	1	PROGRAMMING LABEL		
	59313-91999	1	BINS, OPERATING AND SERVICE MANUAL		59313-91999
	8120-1395	1	CABLE ASSEMBLY (8 FT)		
	1251-3759	4	ADAPTER: BNC JACK TO TELEPHONE PLUG	28480	1251-3759

See introduction to this section for ordering information

Section VI — Replaceable Parts
Model 59313A

Table 6-3. Replaceable Parts (Continued)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
OPTION NO. 001	47310-60010 47310-60011	1	OPTION 001(FRONT PANEL, WHITE) FRONT PANEL, WHITE DELETE: FRONT PANEL, GRAY	28480	47310-60010
003	8120-1900 8120-1992	1 1	OPTION 003 (30" POWER CORD) CABLE, CEE22-CEE22 DELETE: CABLE ASSEMBLY (8 FT.)	16428	OBD
009	2110-0234 2110-0235	1	OPTION 009 (230V OPERATION) FUSE .1A 250V SLO-BLO 1.25X.25 UL IEC DELETE: FUSE .2A 250V SLO-BLO 1.25X.25 UL IEC	71400	MDL 1/10
030	8120-1996 8120-1992	1	OPTION 030 (30" NEMA/CEE PWR CD) CABLE ASSEMBLY, 30", NEMA TO CEE DELETE: CABLE ASSEMBLY (8 FT.)	16428	OBD
034	07804-00320 2510-0102 78101-25010 2360-0015	1 1 1 2	OPTION 034(MOUNTING, HALF-MODULE) CHANNEL STOP SCREW-MACH 8-32 .375-IN-LG 100 DEG CLIP SCREW-MACH 6-32 1.125-IN-LG RD-HD-SLT	28480 28480 28480 28480	07804-00320 2510-0102 78101-25010 2360-0015
038	8120-2133 8120-1992	1	OPTION 038(8' PWR CORD, CEE-CEE) CABLE, AC CEE-22(2.4 METERS) DELETE: CABLE ASSEMBLY (8 FT.)	16428	OBD
039	47304-00100 2360-0117 2510-0049 47304-20010 2190-0758 2510-0051 2580-0006	2 4 4 2 4 4 4	OPTION 039(RACK MOUNT FOR SINGLE MODULE, (WHT PAINT ONLY)) RACKING SPACER SCREW-MACH 6-32 .375-IN-LG PAN-HD-POZI 3/8 SCREWS SCREW-MACH 8-32 .5-IN-LG PAN-HD-POZI 1/2 SCREWS RACKING EAR WASHER-FL MTLG NO.-8 .171-IN-ID .5-IN-OD SCREW-MACH 8-32 .625-IN-LG PAN-HD-POZI NUT-HEX-W/LKWR 8-32-THD .125-THK	28480 28480 28480 28480 28480 28480 78189	47304-00100 2360-0117 2510-0049 47304-20010 2190-0758 2510-0051 KEP511-081600-00
090	8120-1351 8120-1992	1	OPTION 090(TUK POWER CORD) CABLE ASSY HGP-JKT DELETE: CABLE ASSEMBLY (8 FT.)	28480	8120-1351
092	8120-1689 8120-1992	1	OPTION 092 (W EUROPEAN PWR CORD) CABLE ASSY 3-COND DELETE: CABLE ASSEMBLY (8 FT.)	0007K	402 311

Section VI — Replaceable Parts
Model 59313A

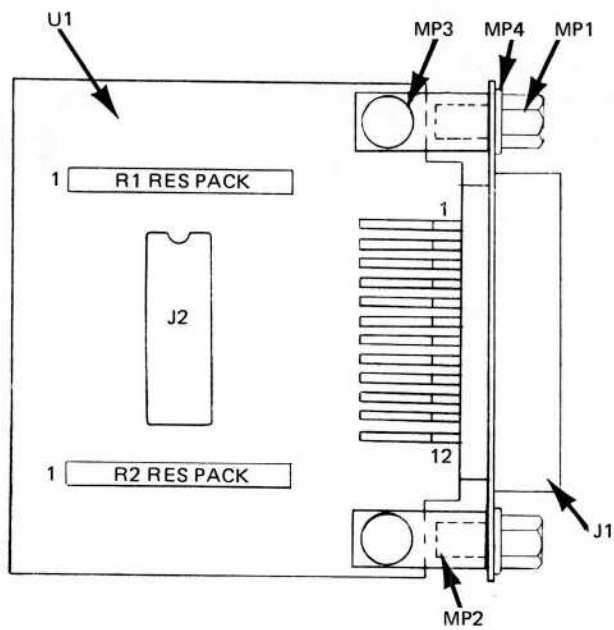


Figure 6-5. Component Locations, Interface PC Assembly A1A2A1

Section VI — Replaceable Parts
Model 59313A

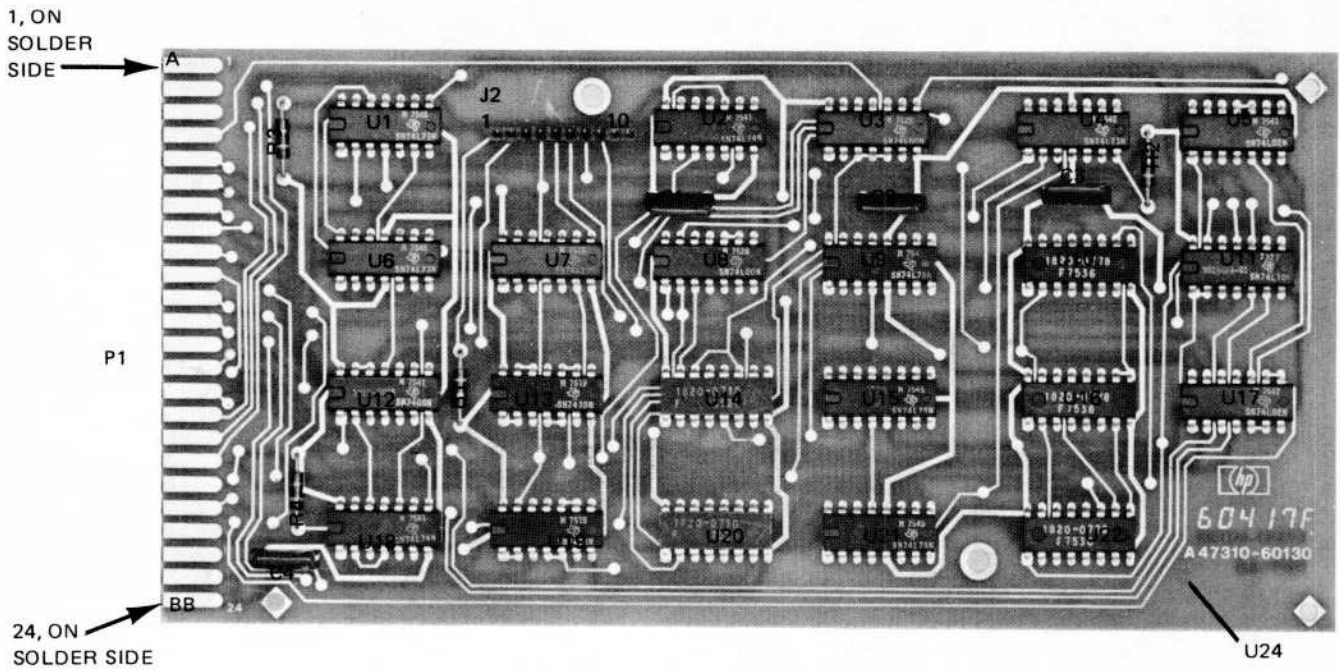


Figure 6-7. Component Locations, Middle PC Assembly A3

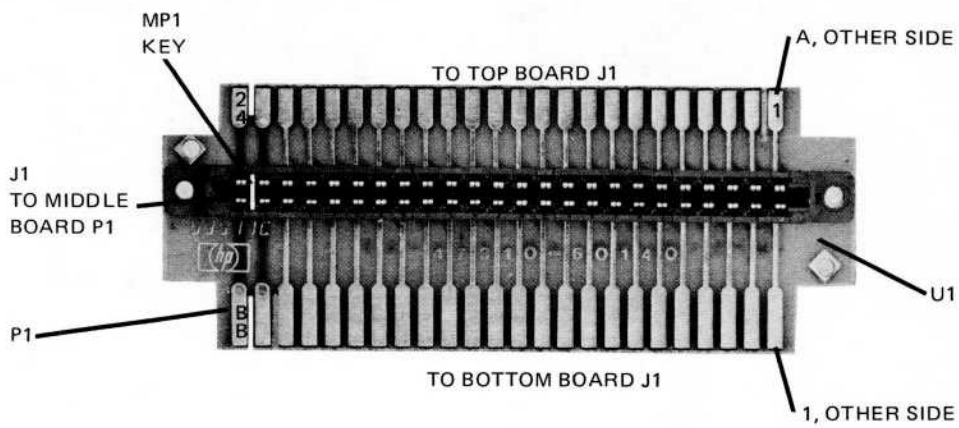


Figure 6-8. Component Locations, Bottom PC Assembly A4

Section VI — Replaceable Parts
 Model 59313A

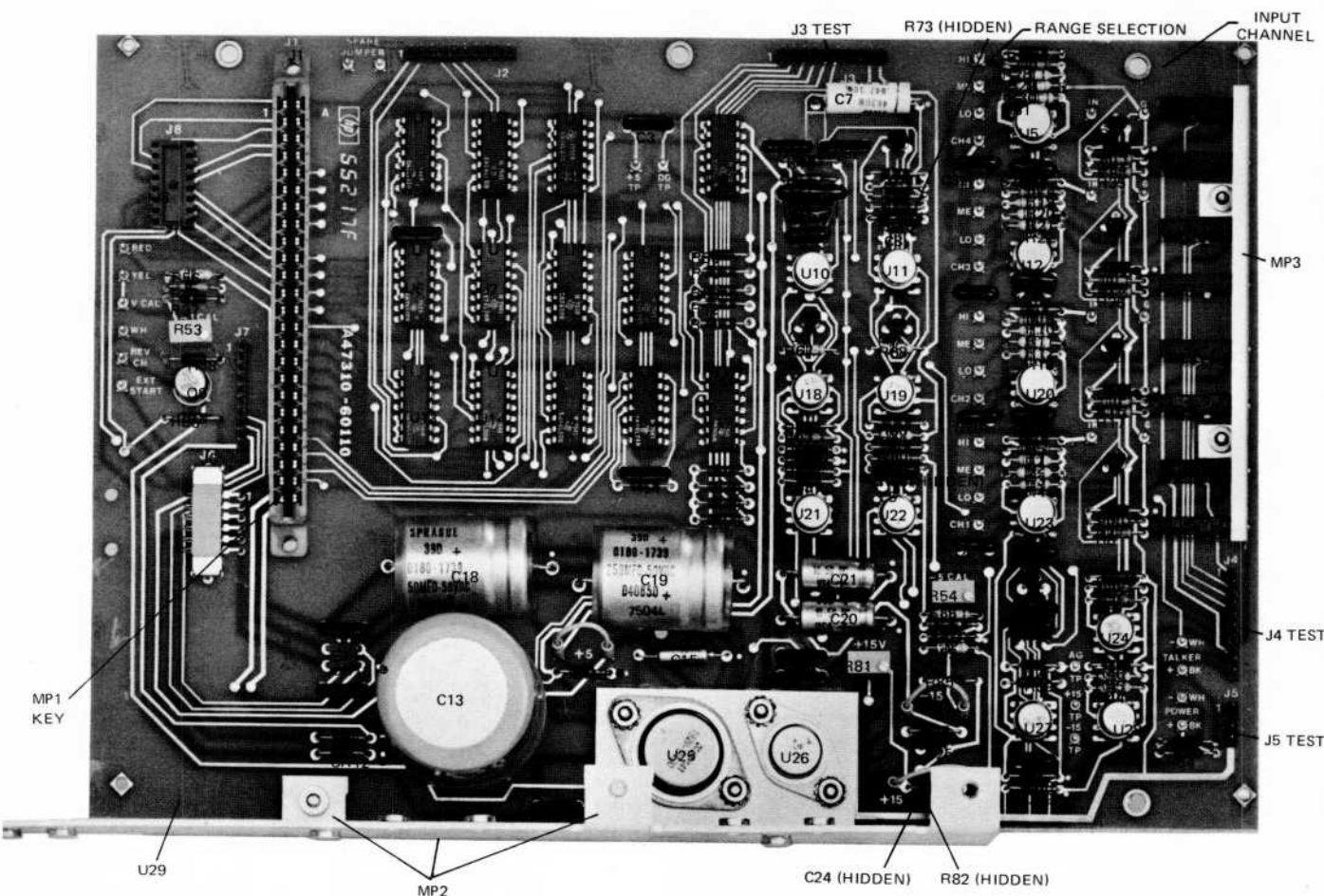
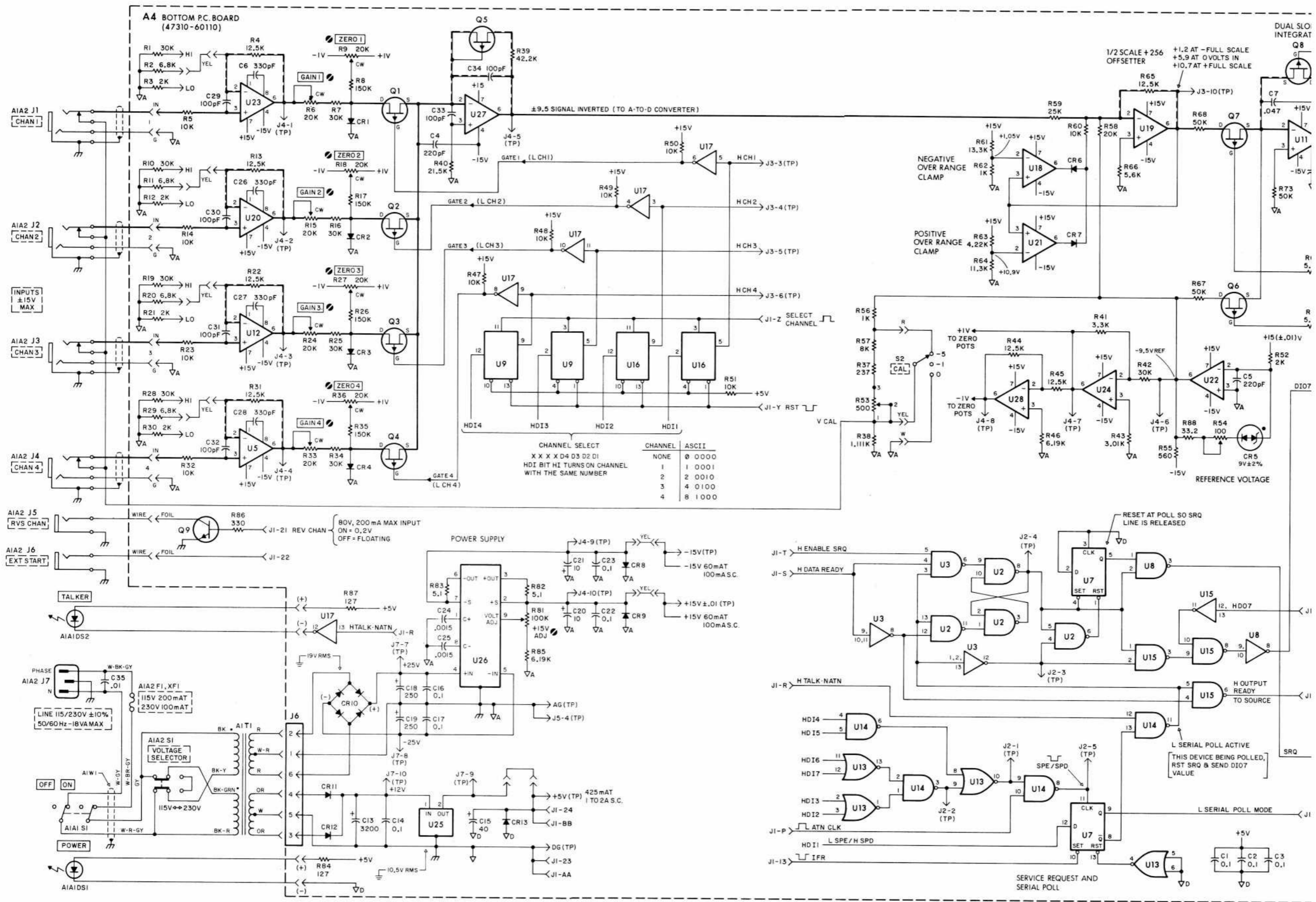
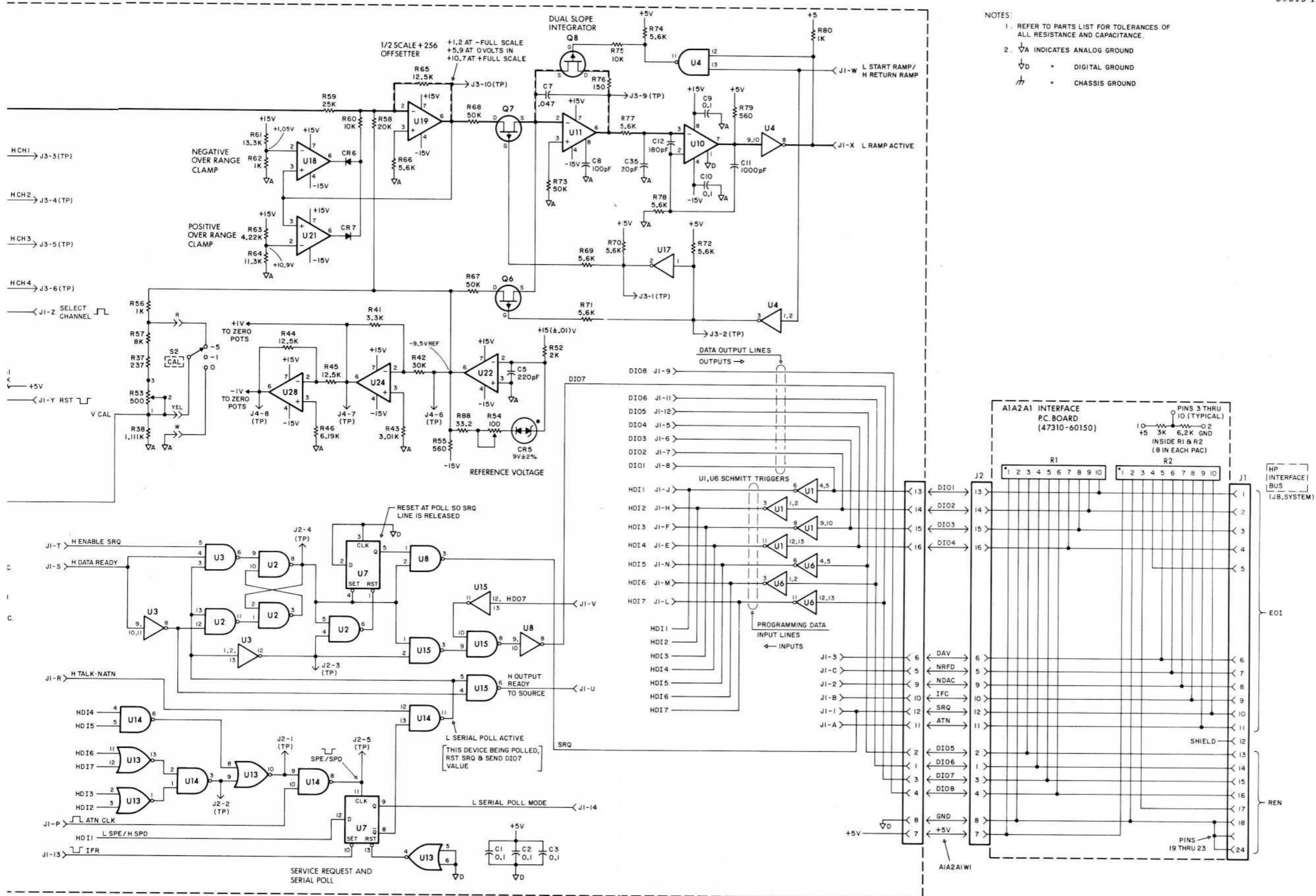


Figure 6-9. Component Locations, Interconnection PC Assembly A5





- NOTES:
1. REFER TO PARTS LIST FOR TOLERANCES OF ALL RESISTANCE AND CAPACITANCE.
 2. ∇ A INDICATES ANALOG GROUND
 ∇ D = DIGITAL GROUND
 ∇ = CHASSIS GROUND

Figure 6-10 Schematic Diagram, Bottom Board A4

Section VI – Replaceable Parts
 Model 59313A
 59313-1

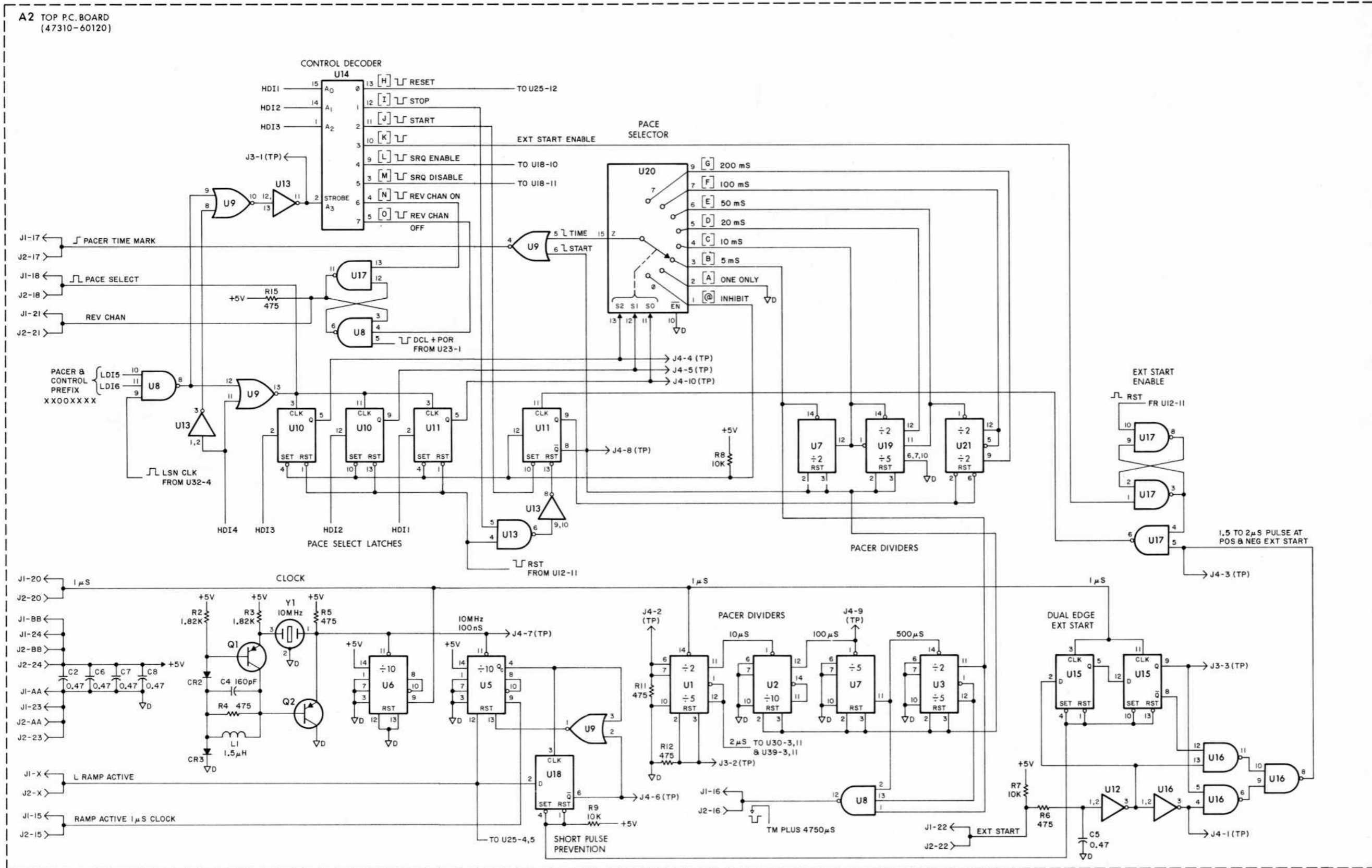


Figure 6-11. Schematic Diagram, Top Board A2

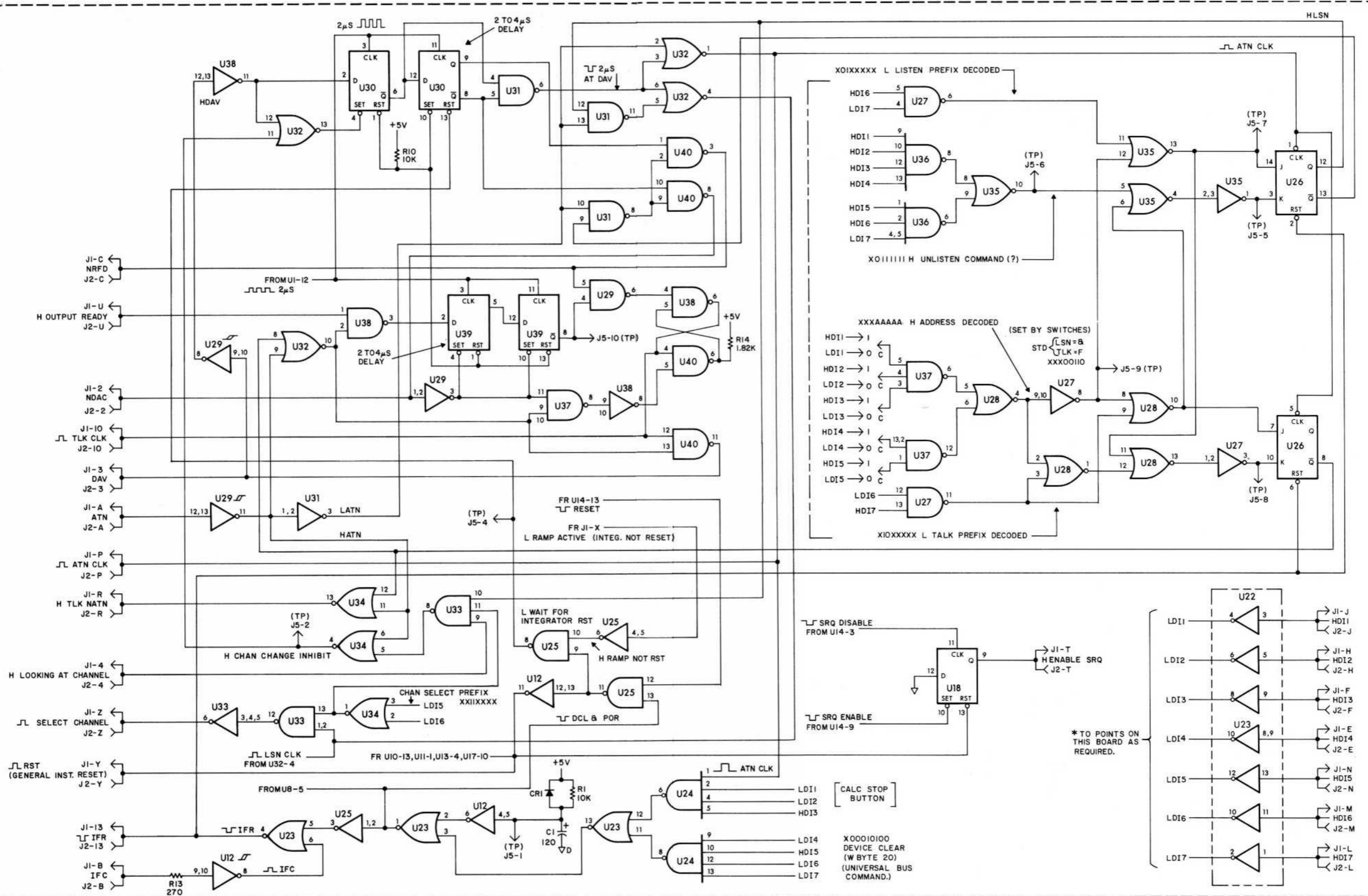


Figure 6-11. Schematic Diagram, Top Board A2 (Continued)

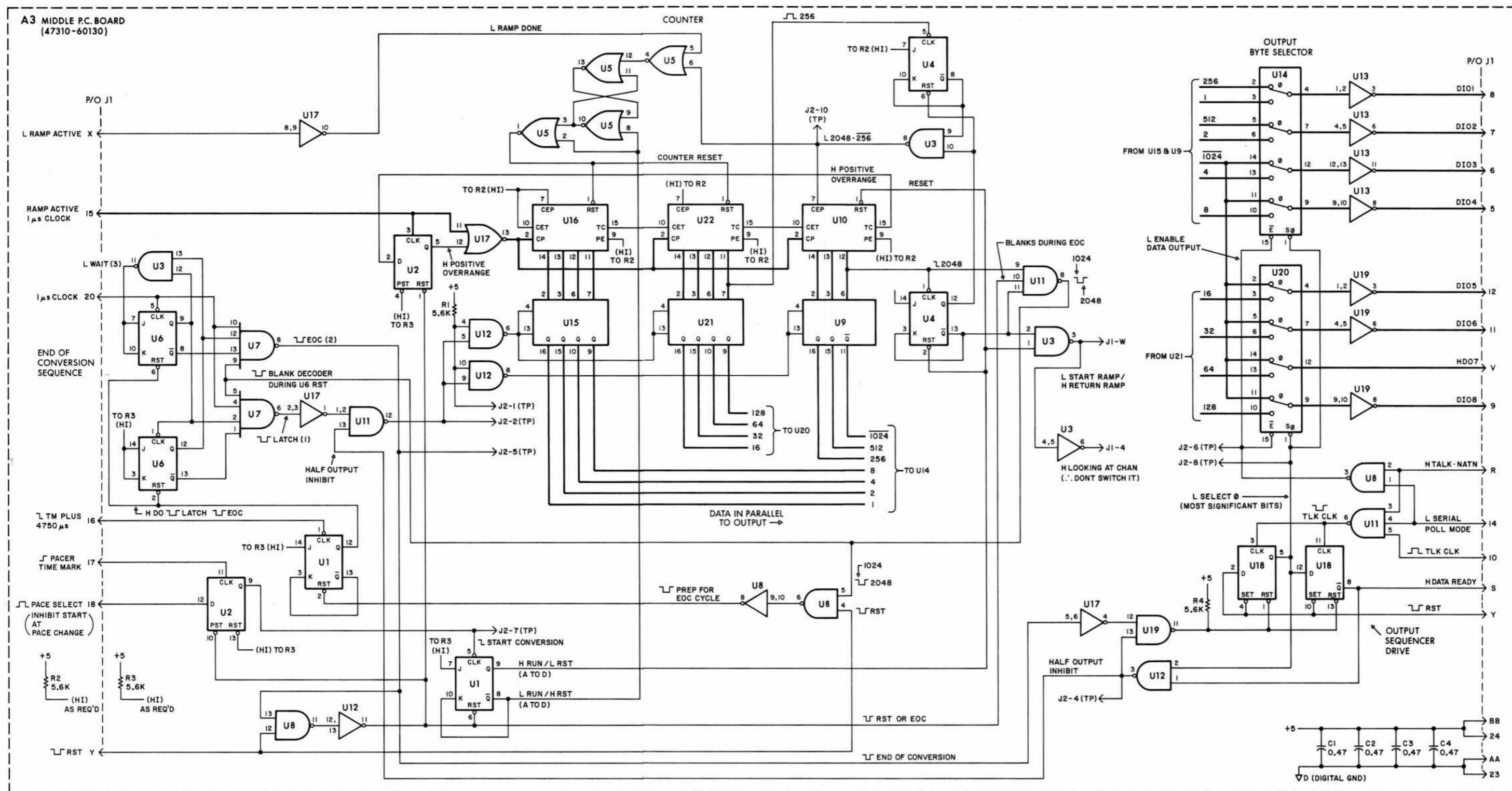


Figure 6-12 Schematic Diagram, Middle Board A3

APPENDIX I THE HP INTERFACE BUS

The HP Interface Bus transfers data and commands between the components of an instrumentation system on 16 signal lines. The interface functions for each system component are performed within the component so only passive cabling is needed to connect the system. The cables connect all instruments, controllers, and other components of the system in parallel to the signal lines.

Eight of the lines (DI01-DI08) are reserved for the transfer of data and other messages in a byte-serial, bit-parallel manner. Data and message transfer is asynchronous, coordinated by the three handshake lines (DAV, NRFD, NDAC). The other five lines are for control of bus activity. Figure A1 shows the lines.

Devices connected to the bus may be talkers, listeners, or controllers. The controller dictates the role of each of the other devices by setting the ATN (attention) line true and sending talk or listen addresses on the data lines (DI01-DI08). Addresses are set into each device at the time of system configuration either by switches built into the device or by jumpers on a PC board. While the ATN line is true, all devices must listen to the data lines. When the ATN line is false, only devices that have been addressed will actively send or receive data. All others ignore the data lines.

Several listeners can be active simultaneously but only one talker can be active at a time. Whenever a talk address is put on the data lines (while ATN is true), all other talkers will be automatically unaddressed.

Information is transmitted on the data lines under sequential control of the three handshake lines. No step in the sequence can be initiated until the previous step is completed. Information transfer can proceed as fast as devices can respond, but no faster than allowed by the slowest device presently addressed as active. This permits several devices to receive the same message byte concurrently.

The ATN line is one of the five control lines. When ATN is true, addresses and universal commands are transmitted on only seven of the data lines using the ASCII code*. When ATN is false, any code of 8 bits or less understood by both talker and listener(s) may be used.

The other control lines are IFC, REN, SRQ, EOI.

IFC (interface clear) places the interface system in a known quiescent state.

REN (remote enable) is used with other coded messages to select either local or remote control of each device.

Any active device can set the SRQ (service request) line true. This indicates to the controller that some device on the bus wants attention, say a counter that has just completed a time-interval measurement and wants to transmit the reading to a printer.

EOI (end or identify) is used by a device to indicate the end of a multiple-byte transfer sequence. When a controller sets both the ATN and EOI lines true, each device capable of a parallel poll indicates its current status on the DIO line assigned to it.

In the interest of cost-effectiveness it is not necessary for every device to be capable of responding to all the lines. Each can be designed to respond only to those lines that are pertinent to its function on the bus.

The operation of the interface is generally controlled by one device equipped to act as controller. It uses a group of commands to direct the other instruments on the bus in carrying out their functions of talking and listening.

*American Standard Code for Information Interchange.

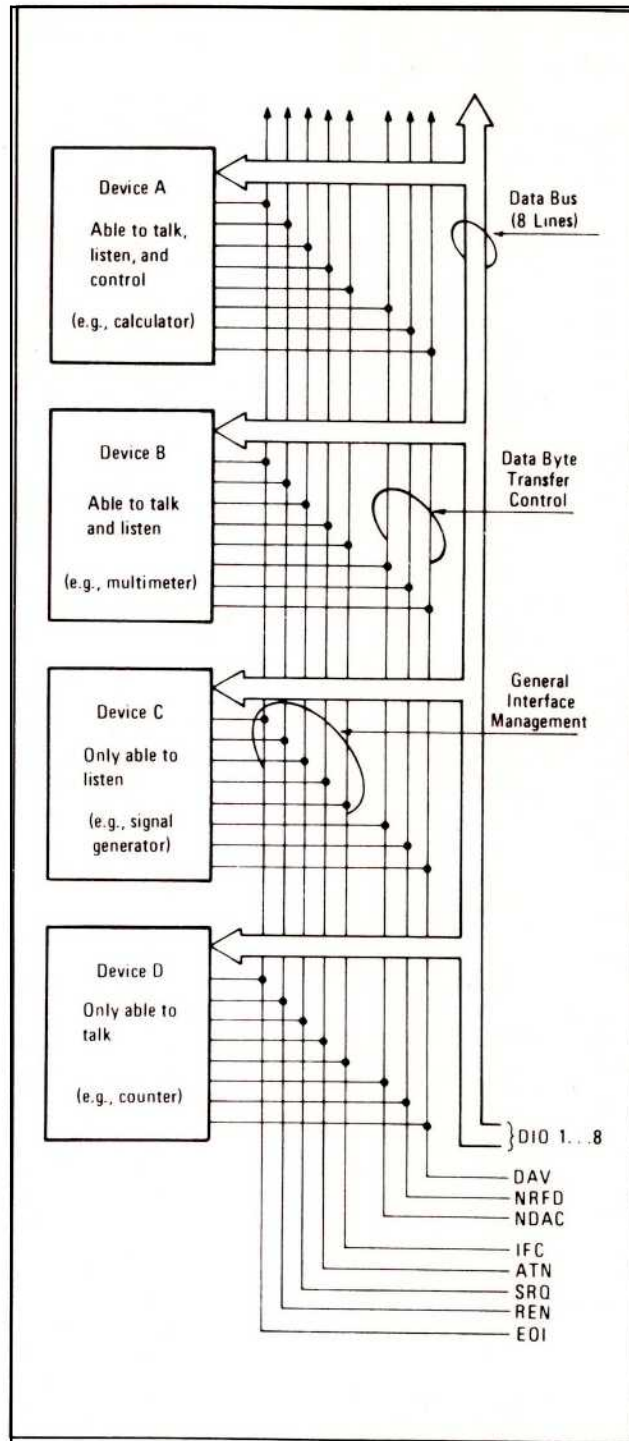


Figure A-1. Bus Signal Lines

The controller has two ways of sending interface messages. Multiline messages, which cannot exist concurrently with other multiline messages, are sent over the eight data lines and the three transfer-bus lines. Uniline messages are transferred over the five individual lines of the management bus.

The commands serve several different purposes:

(1) *Addresses*, or talk and listen commands, select the instruments that will transmit and accept data. They are all multiline messages.

(2) *Universal commands* cause every instrument equipped to do so to perform a specific interface operation. They include multiline messages and three uniline commands, interface clear (IFC), remote enable (REN), and attention (ATN).

(3) *Addressed commands* are similar to universal commands, except that they affect only those devices that are addressed and are all multiline commands. An instrument responds to an addressed command, however, only after an address has already told it to be a talker or listener.

(4) *Secondary commands* are multiline messages that are always used in series with an address, universal command, or addressed command (also referred to as primary commands) to form a longer version of each. Thus they extend the code space when necessary.

To address an instrument, the controller uses seven of the eight data-bus lines. This allows instruments using the ASCII 7-bit code to act as controllers. As shown in Table A1, five data bits are available for addresses, so a total of 31 addresses is available in one byte. If all secondary commands are used to extend this into a two-byte addressing capability, 961 addresses become available (31 addresses in the second byte for each of the 31 in the first byte).

Table A1. Command and Address Codes

Code Form							Meaning
X	0	0	A ₅	A ₄	A ₃	A ₂ A ₁	Universal Commands Listen Addresses
X	0	1	A ₅	A ₄	A ₃	A ₂ A ₁	
except							
X	0	1	1	1	1	1	Unlisten Command
X	1	0	A ₅	A ₄	A ₃	A ₂ A ₁	Talk Addresses
except							
X	1	0	1	1	1	1	Untalk Command
X	1	1	A ₅	A ₄	A ₃	A ₂ A ₁	Secondary Commands
except							
X	1	1	1	1	1	1	Ignored
(Code used when attention (ATN) is true (low))							

NOTES

**APPENDIX II
CONVERSION TECHNIQUES**

A. TWO'S COMPLEMENT BINARY TO DECIMAL AND DECIMAL TO TWO'S COMPLEMENT BINARY CONVERSION.

59313A OUTPUT								
Bus Data Lines →	DIO8	DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DI01
1ST BYTE →	BIT 11	BIT 11	BIT 11	BIT 11	BIT 11	BIT 11	BIT 10	BIT 9
2ND BYTE →	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1

BIT 1 = LEAST SIGNIFICANT BIT.
BIT 11 = MOST SIGNIFICANT BIT = SIGN BIT

Data on the bus lines is sent LO = TRUE; however, for this discussion the convention will be:

1 = HI = TRUE
0 = LO = FALSE

B. CONVERTING THE TWO'S COMPLEMENT OUTPUT TO DECIMAL.

1. Examine sign bit (Bit 11).

If a zero, then go to Step 2.

If a one, then go to Step 3.

2. Convert the string of ones and zeros to a decimal number using the following formula: (Note 1)

$$N = (1 * \text{BIT } 1) + (2 * \text{BIT } 2) + (4 * \text{BIT } 3) + (8 * \text{BIT } 4) + (16 * \text{BIT } 5) + (32 * \text{BIT } 6) + (64 * \text{BIT } 7) + (128 * \text{BIT } 8) + (256 * \text{BIT } 9) + (512 * \text{BIT } 10)$$

N is the decimal number desired

3. Convert the string of ones and zeros to a decimal number using the following formula: (Notes 1, 2)

$$N = [-1] + [1 * (\text{BIT } 1 - 1)] + [2 * (\text{BIT } 2 - 1)] + [4 * (\text{BIT } 3 - 1)] + [8 * (\text{BIT } 4 - 1)] + [16 * (\text{BIT } 5 - 1)] + [32 * (\text{BIT } 6 - 1)] + [64 * (\text{BIT } 7 - 1)] + [128 * (\text{BIT } 8 - 1)] + [256 * (\text{BIT } 9 - 1)] + [512 * (\text{BIT } 10 - 1)]$$

N is the decimal number desired.

NOTE 1: Where the formula calls for a bit numeral (#), e.g., Bit 4, insert the value of that bit, 0 or 1, and use that value as a decimal number for the calculation.

NOTE 2: * = multiply.

C. CONVERTING DECIMAL TO TWO'S COMPLEMENT:

N = Decimal number to be converted (−1024 to +1023).

1. If N is positive or zero: Go to Step 2.

If N is negative: Add −1 to N; Complement (change 1 to 0 and 0 to 1); all 1 and 0 obtained in Step 2; Go to Step 2.

2. Bit 11 = 0.

Number	Bit
512	10
256	9
128	8
64	7
32	6
16	5
8	4
4	3
2	2
1	1

For each number in the chart, starting with 512 and going in order, perform the following steps:

- (a) Compare number with N.
- (b) If number is greater than N, then that bit = 0; use unchanged N for next step; go to (a).
- (c) If number is equal or less than N, then that bit = 1; also subtract number from N and use the result for the next step; go to (a).

3. Assemble all 1 and 0 with bit 11 at left and bit 1 at right.

**APPENDIX III
 47310A META MESSAGE INFORMATION**

59313A INTERFACE FUNCTIONS	
MNEMONIC	INTERFACE FUNCTION NAME
SH	SOURCE HANDSHAKE
AH	ACCEPTOR HANDSHAKE
T	TALKER
L	LISTENER
SR	SERVICE REQUEST
DC	DEVICE CLEAR

META MESSAGES THE 59313A RECEIVES	
META MESSAGE	59313A RESPONSE
DATA	PROGRAMMING USING 59313A CONTROL CHARACTER SET
CLEAR	CLEAR 59313A
STATUS BYTE	STANDARD BIT 7 STATUS
ABORT	STANDARD RESPONSE

META MESSAGES THE 59313A SENDS	
META MESSAGE	MESSAGE
DATA	A TO D CONVERTER OUTPUT IN 2 BYTES
REQUIRE SERVICE	OUTPUT READY

NOTES

APPENDIX IV
HEWLETT-PACKARD INTERFACE BUS CODE SET

ASCII CODES

(AMERICAN STANDARD CODE FOR INFORMATION INTERCHANGE)

BITS				b ₇ →	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
b ₄ ↓	b ₃ ↓	b ₂ ↓	b ₁ ↓	COLUMN	0	1	2	3	4	5	6	7
				↓ ROW								
0	0	0	0	0	NUL	DLE	SP	Ø	@	P	•	p
0	0	0	1	1	SOH	DC1	!	1	A	Q	a	q
0	0	1	0	2	STX	DC2	"	2	B	R	b	r
0	0	1	1	3	ETX	DC3	#	3	C	S	c	s
0	1	0	0	4	EOT	DC4	\$	4	D	T	d	t
0	1	0	1	5	ENQ	NAK	%	5	E	U	e	u
0	1	1	0	6	ACK	SYN	&	6	F	V	f	v
0	1	1	1	7	BEL	ETB	'	7	G	W	g	w
1	0	0	0	8	BS	CAN	(8	H	X	h	x
1	0	0	1	9	HT	EM)	9	I	Y	i	y
1	0	1	0	10	LF	SUB	*	:	J	Z	j	z
1	0	1	1	11	VT	ESC	+	;	K	[k	{
1	1	0	0	12	FF	FS	,	<	L	\	l	:
1	1	0	1	13	CR	GS	-	=	M]	m	}
1	1	1	0	14	SO	RS	.	>	N	~	n	~
1	1	1	1	15	SI	US	/	?	O	—	o	DEL

	UNIVERSAL COMMANDS	UNLISTEN COMMAND	UNTALK COMMAND	NOT USED
ADDRESS MODE	↑ LISTEN ADDRESS	↑ TALK ADDRESS		
DATA MODE	NOT USED EXCEPT CR, LF AS WORD TERMINATORS	ALL DATA	NOT USED	

NOTES



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