Hewlett-Packard
9830
Computer

Schematic

Contents

Contents (continued)

NOTE

This schematic has been derived through examination of the equipment.
This is not the manufacturer's schematic.

NOTES

- Printed circuit boards are identified by the Assembly Number printed in the foil of the circuit board. The last two digits of the assembly number distinguish each board type, and correspond to the color coding of the board extraction handles.

- This schematic presents the 4KW RAM board-set so the assemblies are identified as 82,83,84. The connectors they plug into remain identified as N22,N23,N24, from the original design for 2KW RAM boards.

- IC locations are identified by a label of the form:
  U <assembly-type> – <enumeration>
  or
  U <assembly-type> – <row-alpha> <column-number>

  A few boards have the IC locations in the foil, these are used for the enumeration if present. For the CPU and tape drive boards the same enumeration as presented in the HP patent and service manual is used. For other boards, a row-column locator is used, with the row specified by a,b,c,.. and the column by 1,2,3,.. starting at the upper left corner.

- The symbol —▪— represents a connector pin. The solid black end is the male side, the white-filled end is the female side.
  Connector pins are identified by a label of the form:
  N <assembly-type> . <pin>

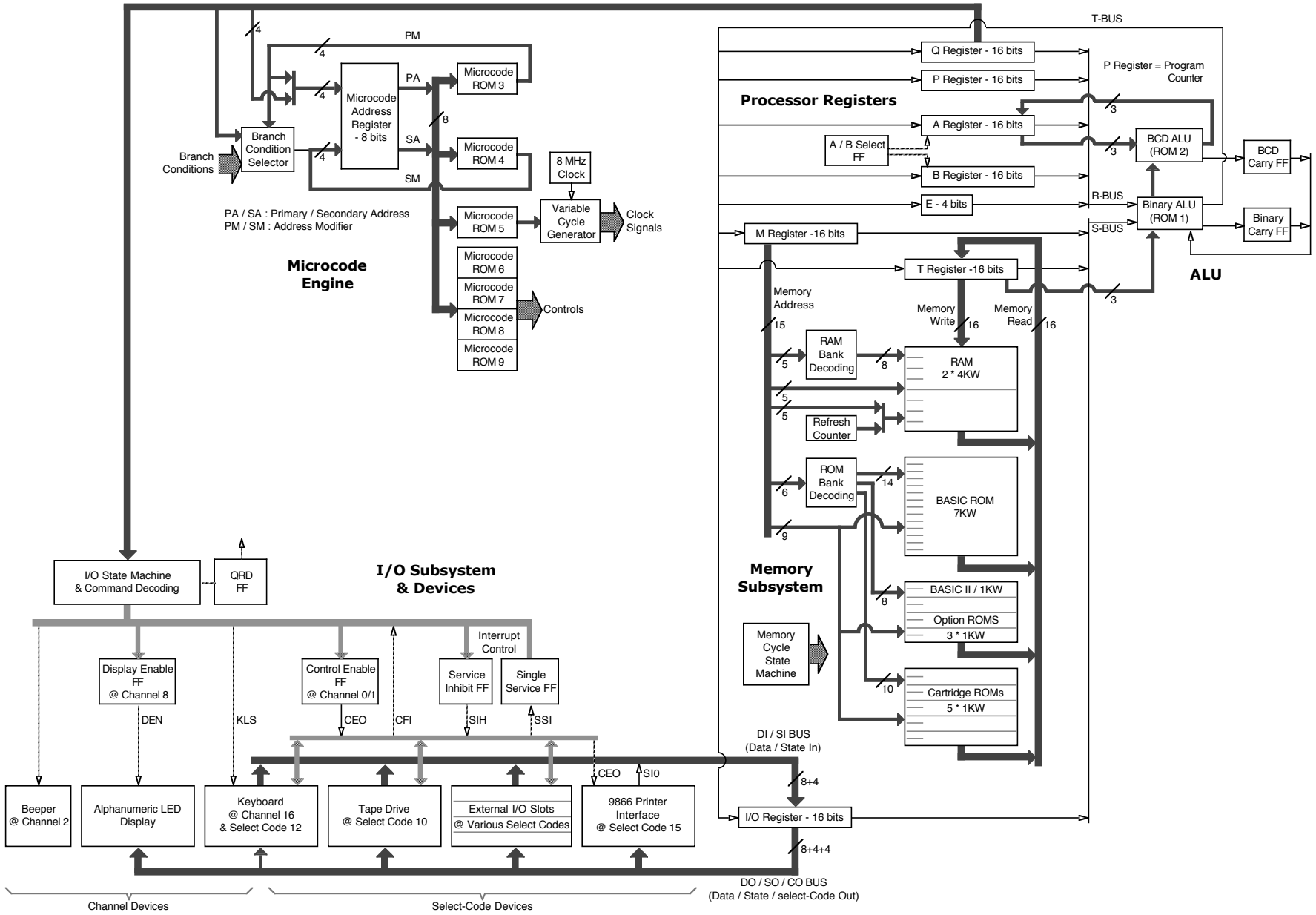
- A small black rectangular marker on the upper half of a gate symbol indicates an open-collector output.

- Capacitance in microfarads unless otherwise noted.

- This schematic is based on a reverse engineering of the 9830 board assemblies listed in the accompanying table, along with some use of the 9830 patent (US #4,012,725) and the tape drive schematics available in the the 9830 service manual.

- 2013 Spring - 2014 Spring: Drawn by bhilpert.
  2014 Oct 02: typo correction nMW75-->nMW15, pg M8.
  2014 Oct 12: corrections to 9866 connector pin labels, pg F2.
  2014 Dec 26: correction, U42-c2.2 to V+5 rather than GND, pg D1.

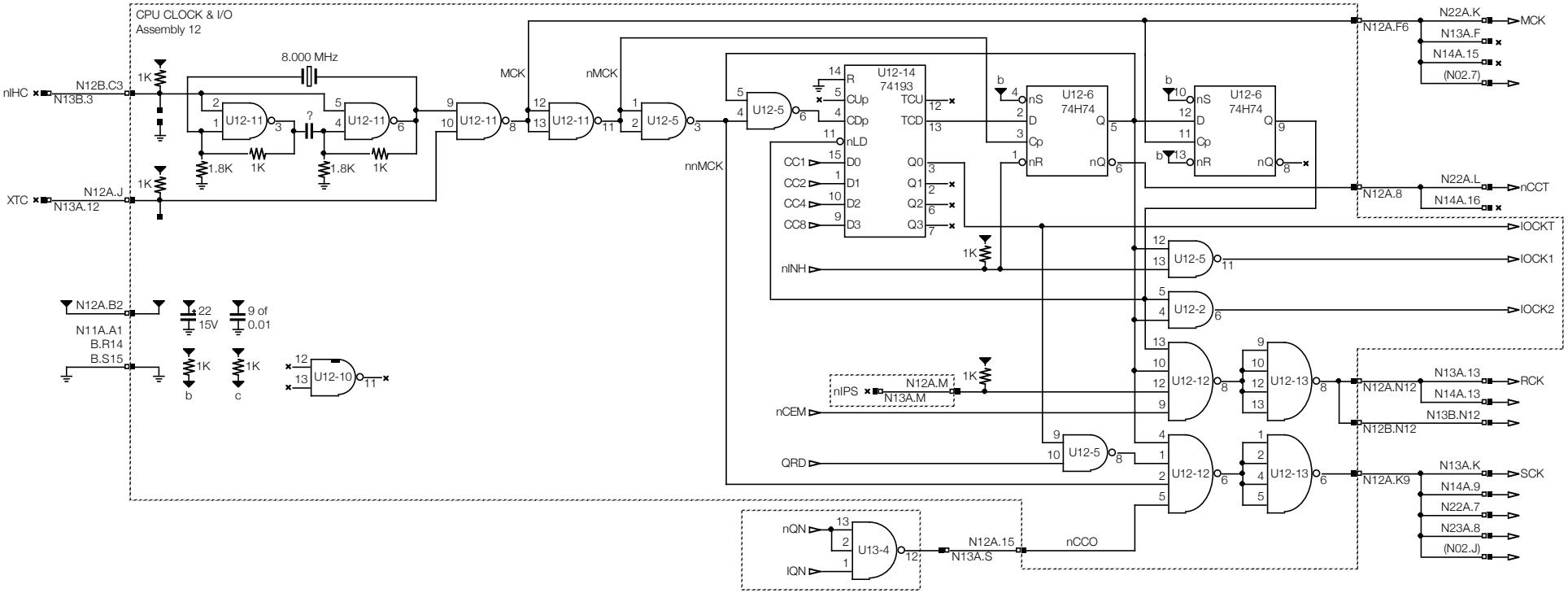
		Unit 1303A00748						Busted 'A' Remnants					
Assembly Name	A #	RE	USE	Foil #	REV	Comp Date	Stamp Date	RE	USE	Foil #	REV	Comp Date	Stamp Date
Backplane	1	*	•	09830-66501	REV B	-	APR 09 1973			-			
External I/O Bus	2	*	•	09830-66502	REV C	7305	APR 13 1973			09830-66502	REV C	7523	-
ROM Cartridge Bus	3	*	•	09830-66503	REV B	7312	APR 16 1973			09830-66503	REV C	7528	-
CPU I/O	11			np		-	-	*	•	09810-66511	REV B	7540	-
CPU Clock & I/O	12			np		-	-	*	•	09810-66512	REV C	7528	-
CPU Microcode Engine	13			np		-	-	*	•	09810-66513	REV A	7536	-
CPU Registers & ALU	14			np		-	-	*	•	09810-66514	REV A	7539	-
BASIC ROM	21			np		-	-	*	•	9830-66521	REV A	7406	-
M Register	82			np		-	-	*	•	09830-66582	REV B	7419	-
T Register	83			np		-	-	*	•	09830-66583	REV A	7313	JUN 05 1973
4KW RAM	84			np		-	-		•	5020-8304	REV A	7419	-
"	84			np		-	-	*	•	5020-8304	REV A	7325	MAY 24 1973
ROM Buffer	25	*	•	09830-66525	REV A	7312	MAR 30 1973			09830-66525	REV B	7536	-
ROM Card	26			np		-	-	*	•	5020-6884	REV A	7532	-
Keyboard Matrix	31	*		09830-66531	REV B	-	-		•	09830-66531	REV B	-	-
Keyboard Encoder	32	*	•	09830-66532	REV D	7649	-			09830-66532	REV D	7537	-
Keyboard Interconnect	34	*	•	09830-26534	REV B	-	-			09830-26534	REV B	-	-
Display	41	*	•	09830-66541	REV D	7452	-			09830-69541	REV E	7511	-
Display Logic	42	*	•	09830-66542	REV A	7308	MAR 30 1973			np		-	-
Power Supply	51			09830-66551	REV A	7308	-	*	•	09830-66551	REV A	7526	-
Tape Interface	61	* M	•	09830-66561	-	7307	APR 17 1973			09830-66561		7531	-
Tape Control	62	* M	•	09865-66562	REV B	7309	MAR 24 1973			np		-	-
Tape R/W	63	* M	•	09865-66563	REV C	7313	APR 11 1973			09865-66563	REV D	7408	DEC 12 1973
Tape Motor Control	64	* M	•	09865-66564	REV B	7311	APR 24 1973			np		-	-
Tape Interconnect	65	*	•	09830-66565	REV B	7405	JAN 17 1974			np		-	-
Tape Head Amp	66	*	•	09865-66566	REV B	7349	-			np		-	-



HP 9830 Computer

Section: Block Diagram

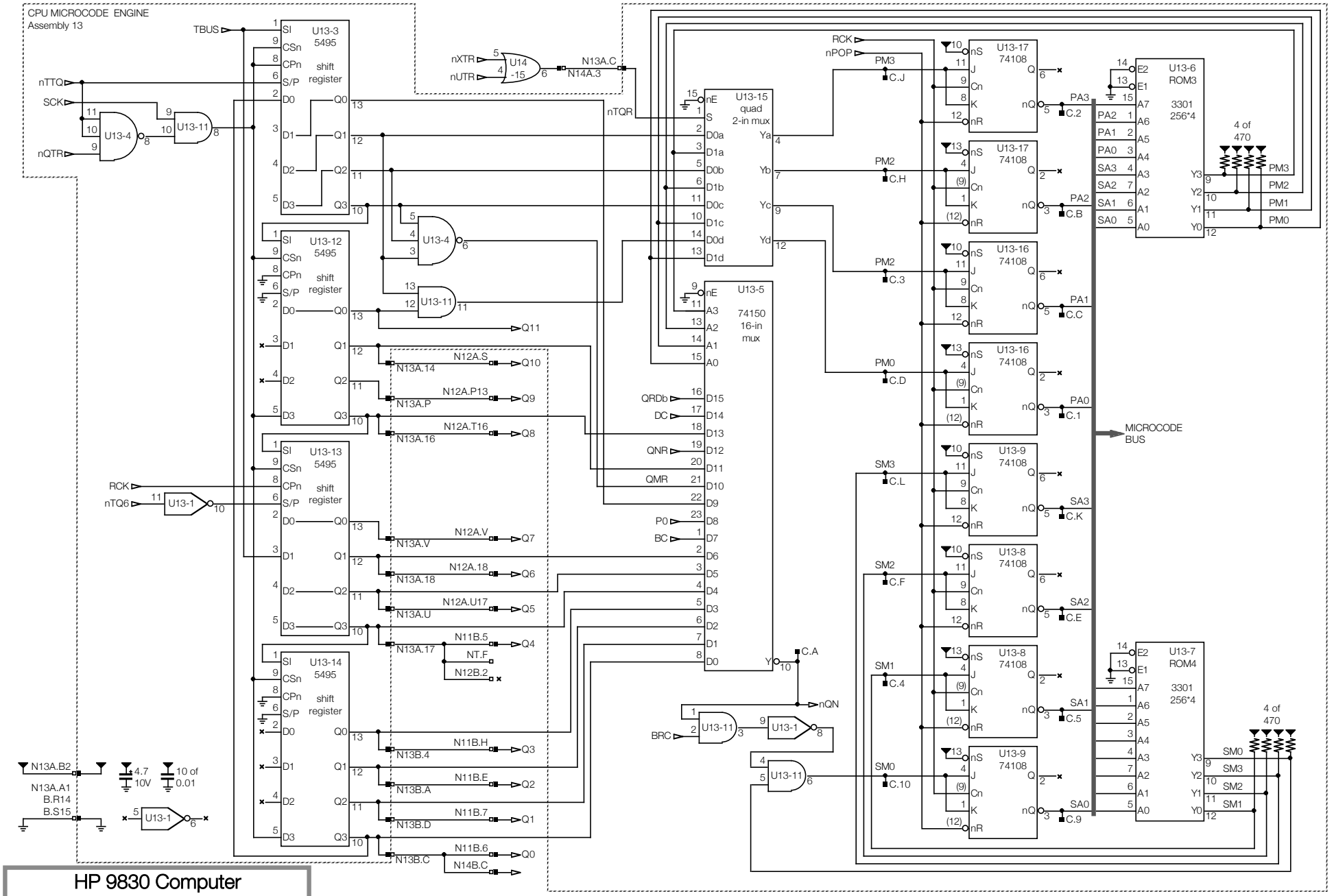
Page: N3 Rendition: 2014 Dec 26



HP 9830 Computer

Section: CPU Clock

Page: P1 Rendition: 2014 Dec 26



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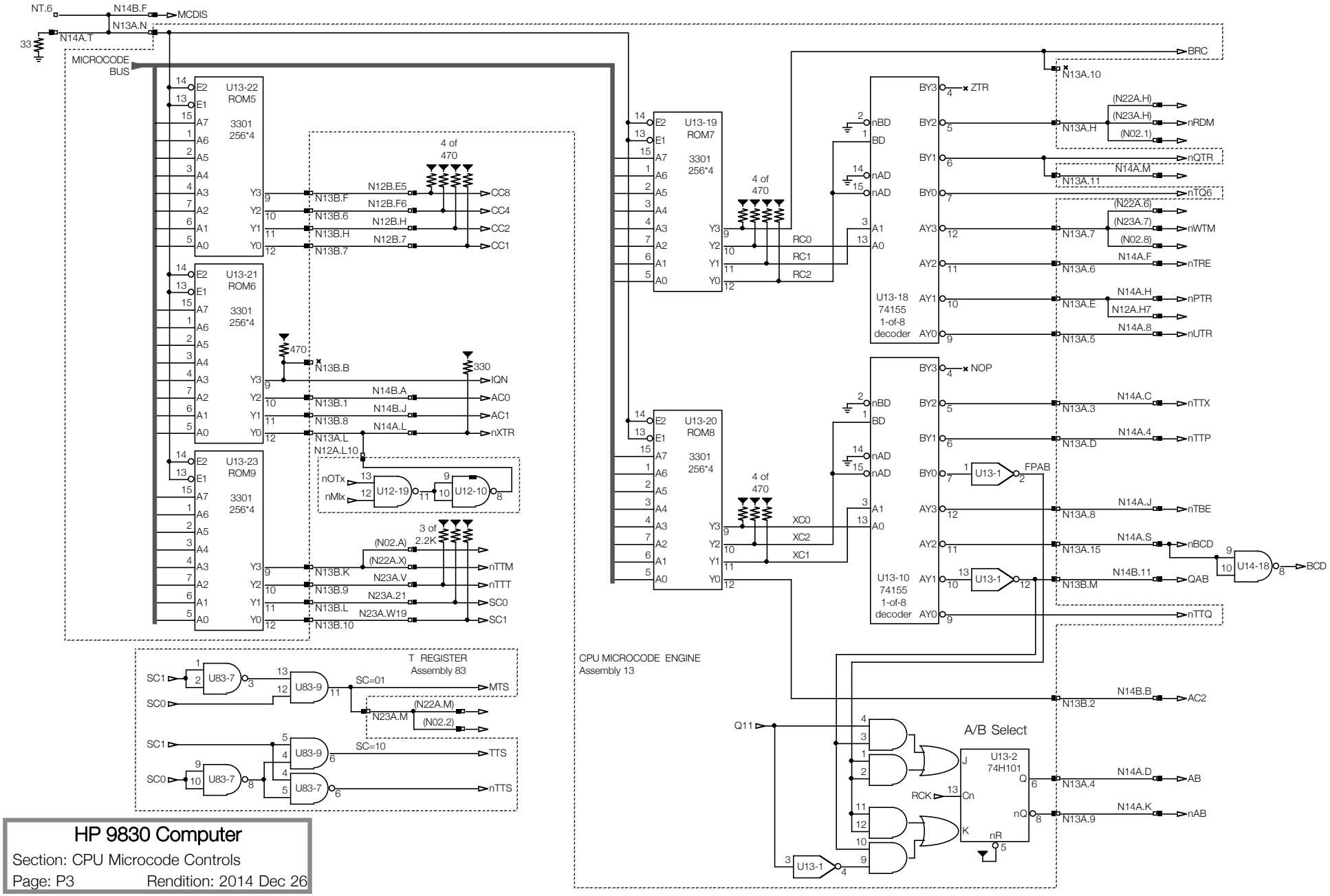
Section: CPU Microcode Sequencing

Page: P2 Rendition: 2014 Dec 26



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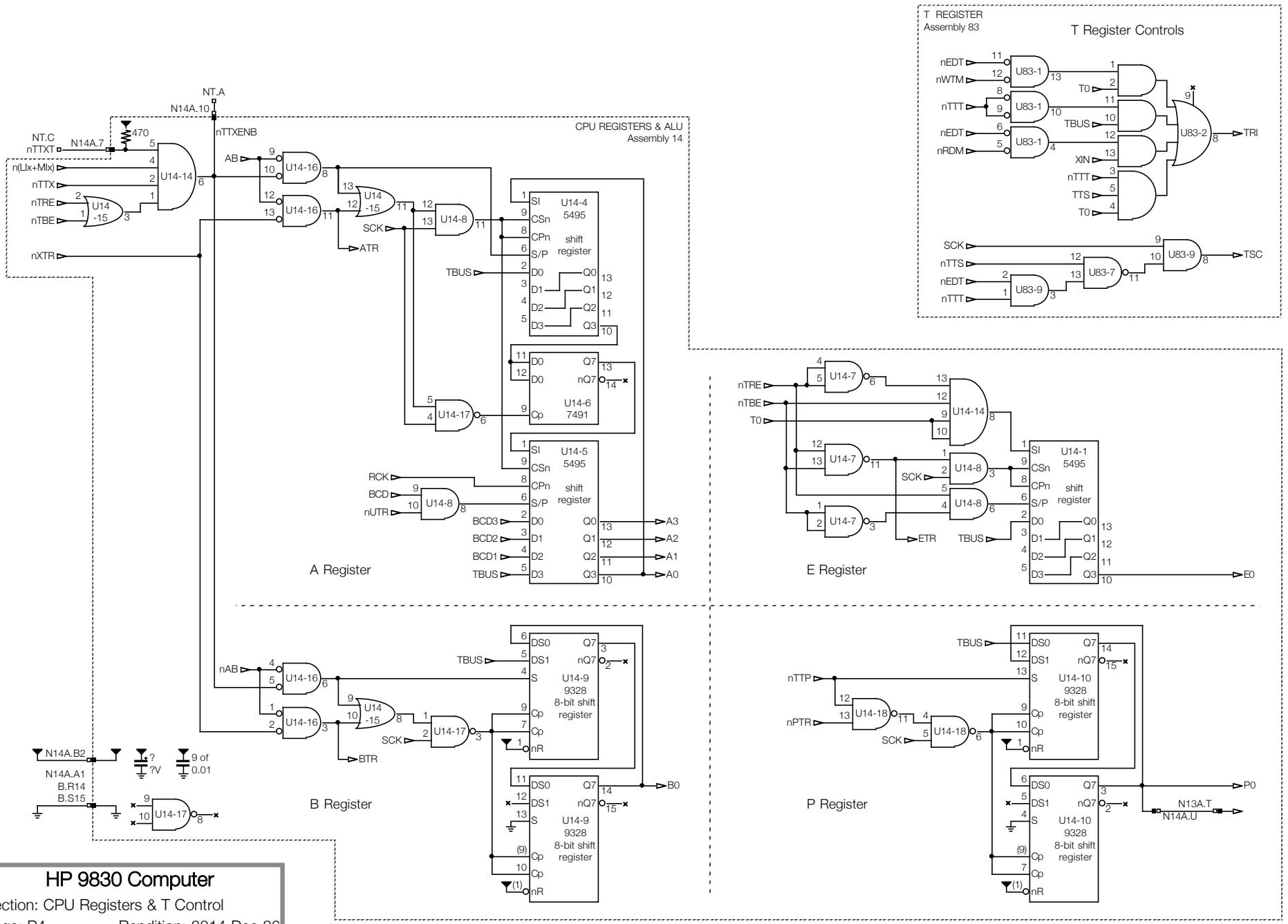
Section: CPU Microcode Controls

Page: P3 Rendition: 2014 Dec 26



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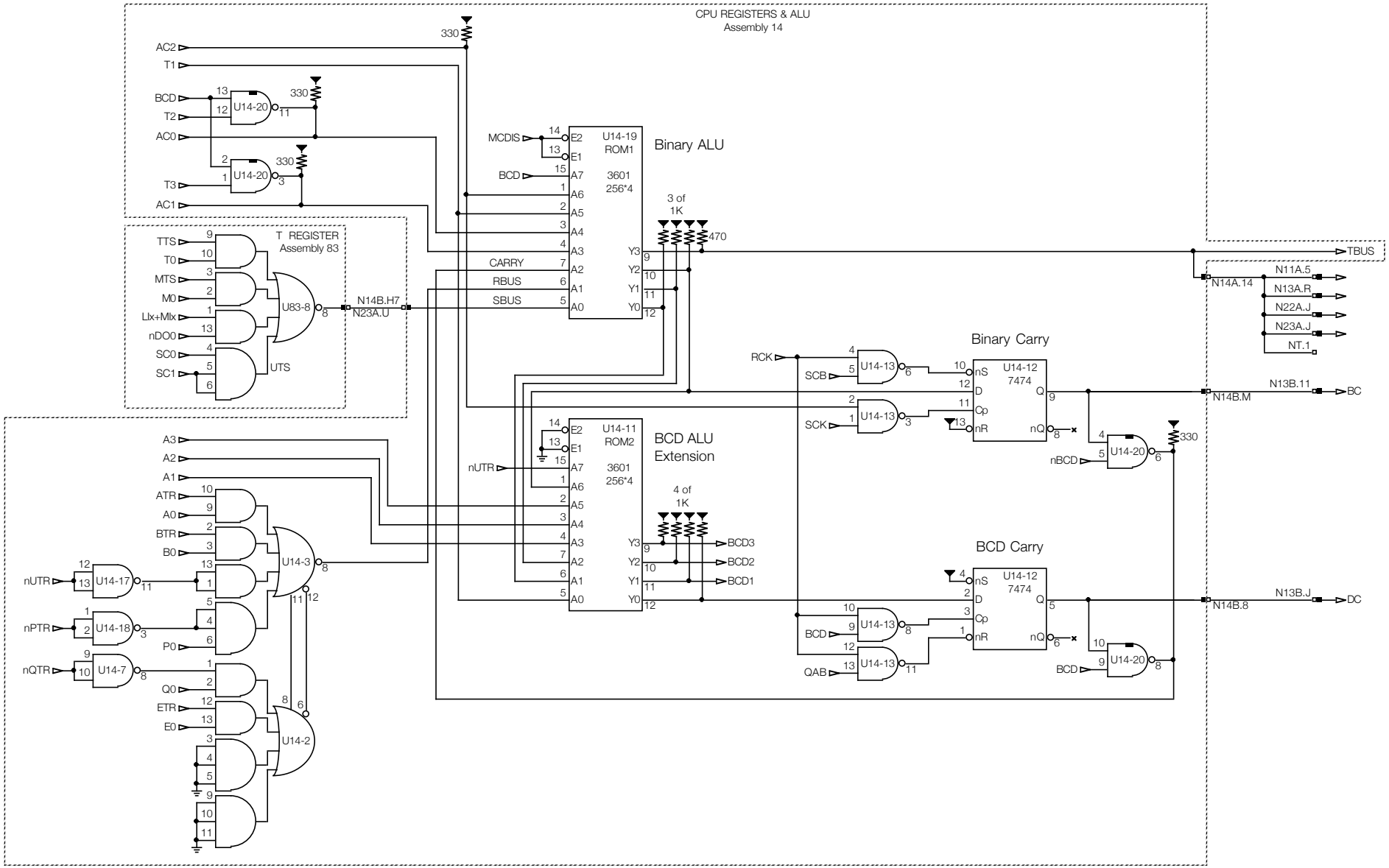
Section: CPU Registers & T Control

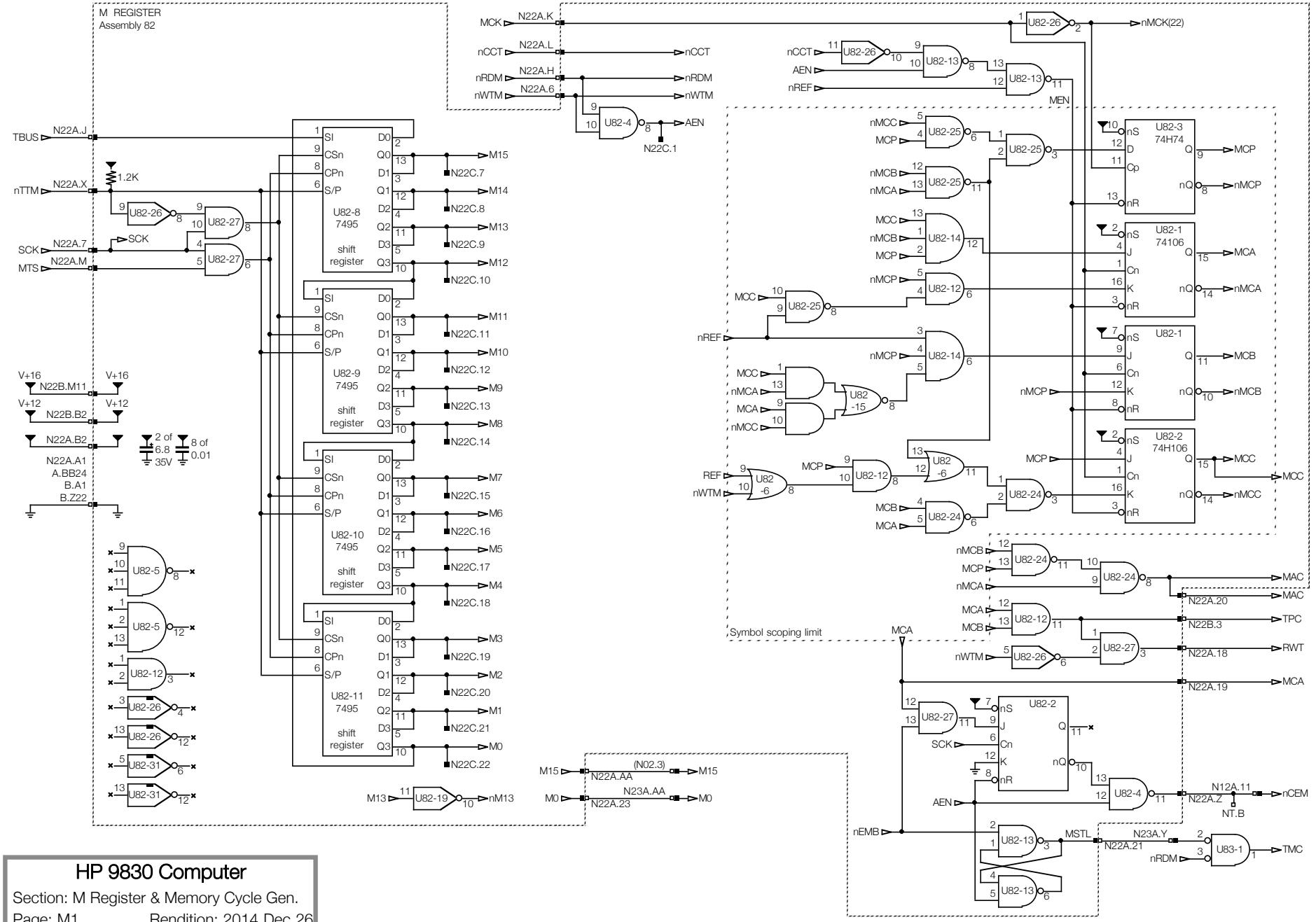
Page: P4 Rendition: 2014 Dec 26



HP 9830 Computer

Section: CPU ALU

Page: P5 Rendition: 2014 Dec 26



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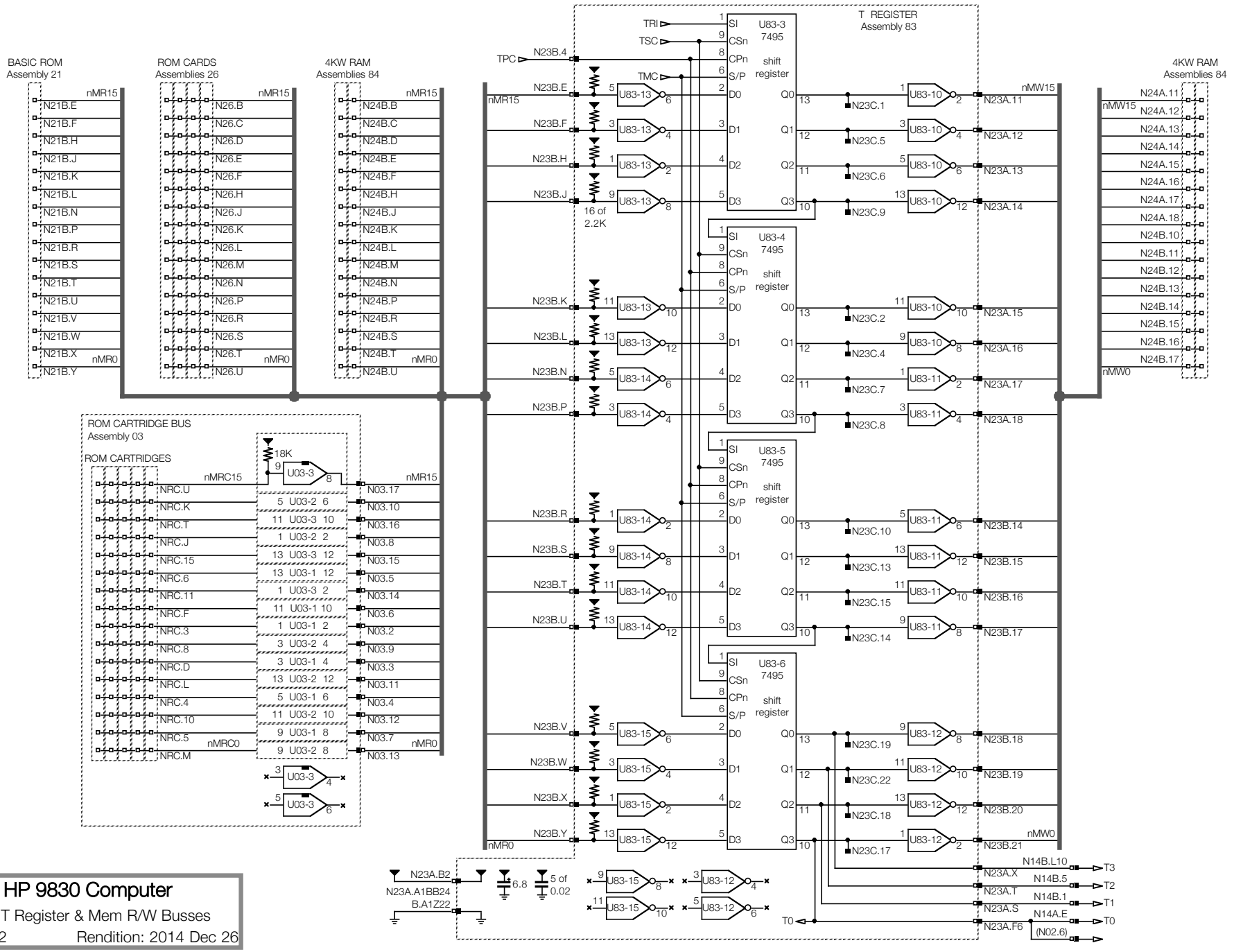
Section: M Register & Memory Cycle Gen.

Page: M1 Rendition: 2014 Dec 26



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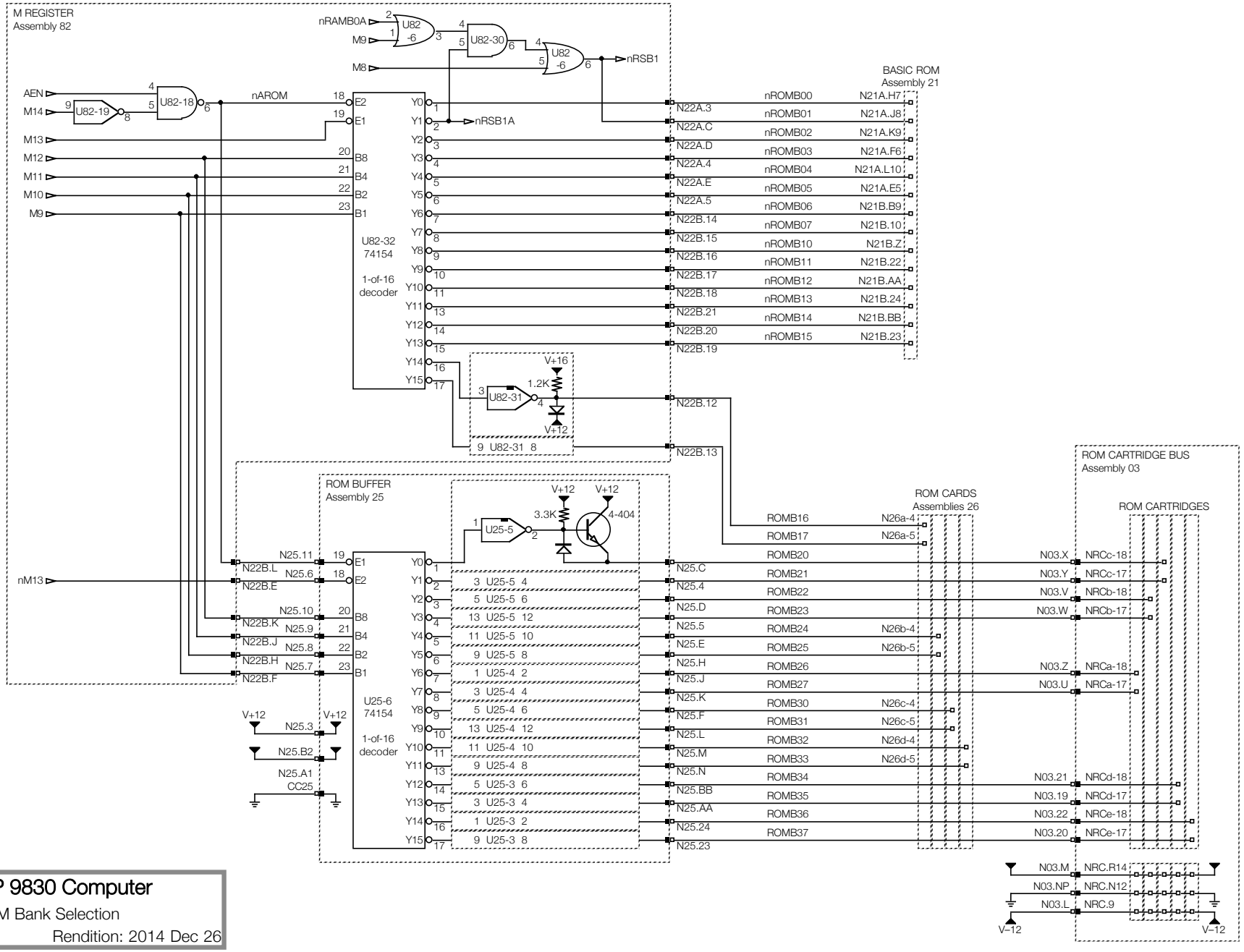
Section: T Register & Mem R/W Busses

Page: M2 Rendition: 2014 Dec 26



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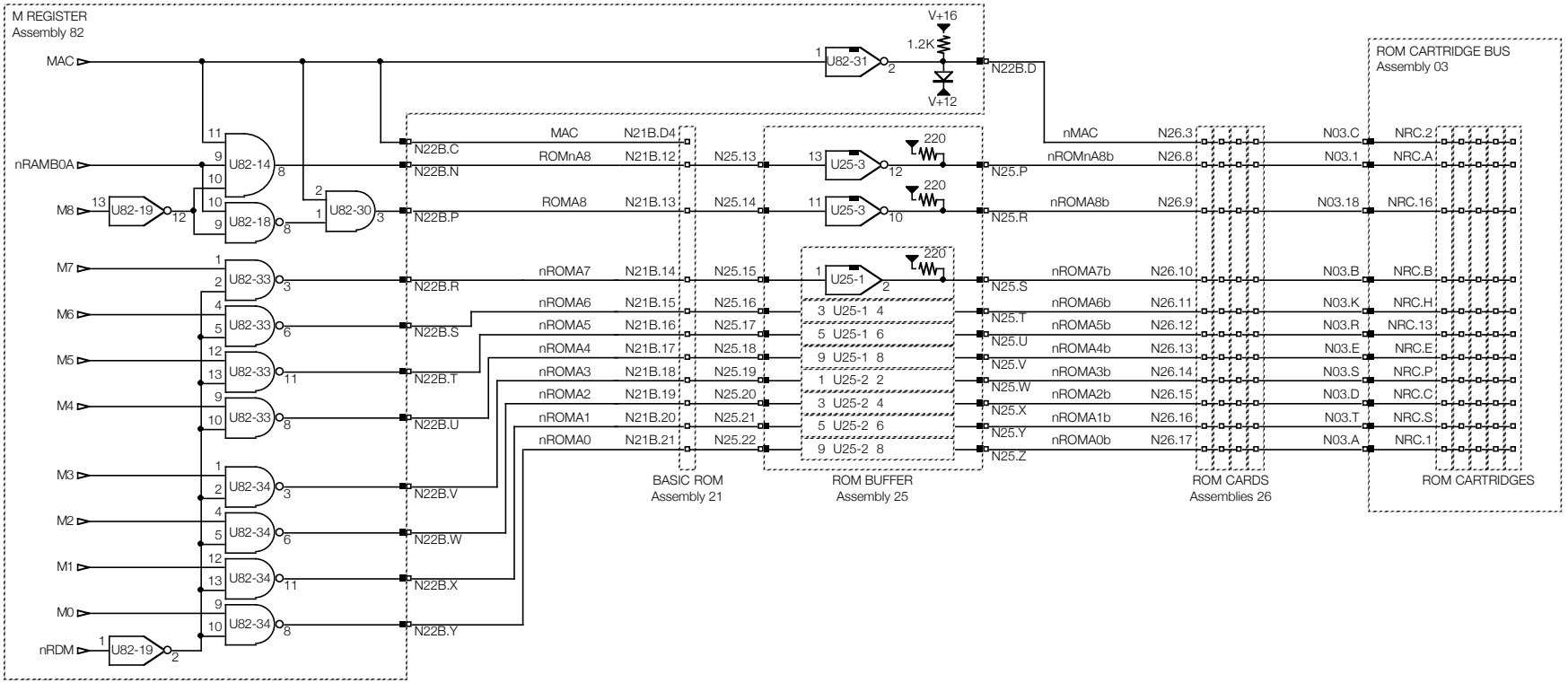
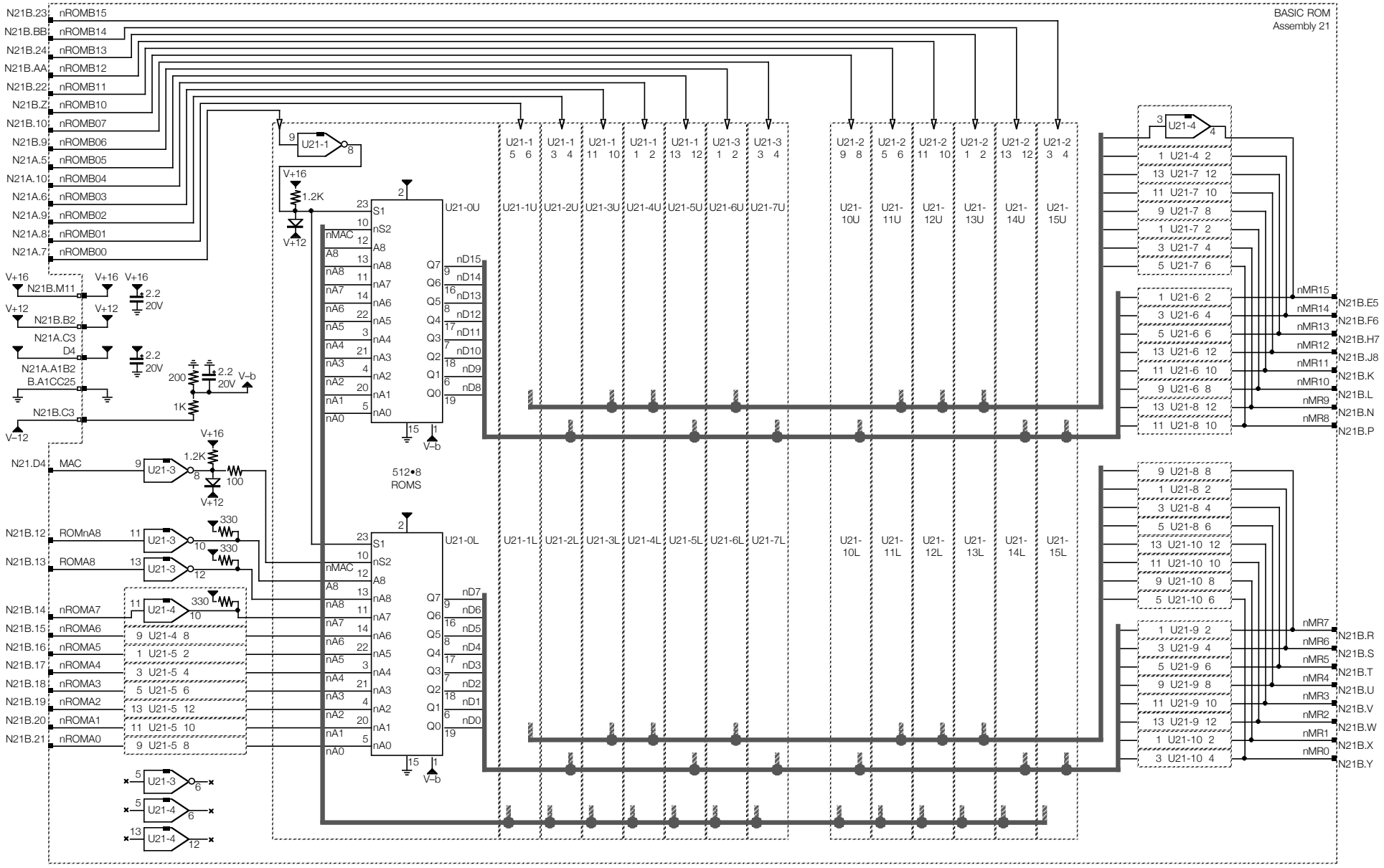
Section: ROM Bank Selection

Page: M3 Rendition: 2014 Dec 26


M REGISTER
Assembly 82
MAC
nRAMB0A
M8
M7
M6
M5
M4
M3
M2
M1
M0
nRDM
U82-14
U82-18
U82-19
U82-30
U82-31
U82-33
U82-34
V+16
1.2K
V+12
N22B.D
N22B.C
N22B.N
N22B.P
N22B.R
N22B.S
N22B.T
N22B.U
N22B.V
N22B.W
N22B.X
N22B.Y
MAC
ROMnA8
ROMA8
nROMA7
nROMA6
nROMA5
nROMA4
nROMA3
nROMA2
nROMA1
nROMA0
N21B.D4
N21B.12
N21B.13
N21B.14
N21B.15
N21B.16
N21B.17
N21B.18
N21B.19
N21B.20
N21B.21
BASIC ROM
Assembly 21
N25.13
N25.14
N25.15
N25.16
N25.17
N25.18
N25.19
N25.20
N25.21
N25.22
U25-3
U25-1
U25-1 4
U25-1 6
U25-1 8
U25-2 2
U25-2 4
U25-2 6
U25-2 8
220
ROM BUFFER
Assembly 25
N25.P
N25.R
N25.S
N25.T
N25.U
N25.V
N25.W
N25.X
N25.Y
N25.Z
nMAC
nROMnA8b
nROMA8b
nROMA7b
nROMA6b
nROMA5b
nROMA4b
nROMA3b
nROMA2b
nROMA1b
nROMA0b
N26.3
N26.8
N26.9
N26.10
N26.11
N26.12
N26.13
N26.14
N26.15
N26.16
N26.17
ROM CARDS
Assemblies 26
ROM CARTRIDGE BUS
Assembly 03
N03.C
N03.1
N03.18
N03.B
N03.K
N03.R
N03.E
N03.S
N03.D
N03.T
N03.A
NRC.2
NRC.A
NRC.16
NRC.B
NRC.H
NRC.13
NRC.E
NRC.P
NRC.C
NRC.S
NRC.1
ROM CARTRIDGES



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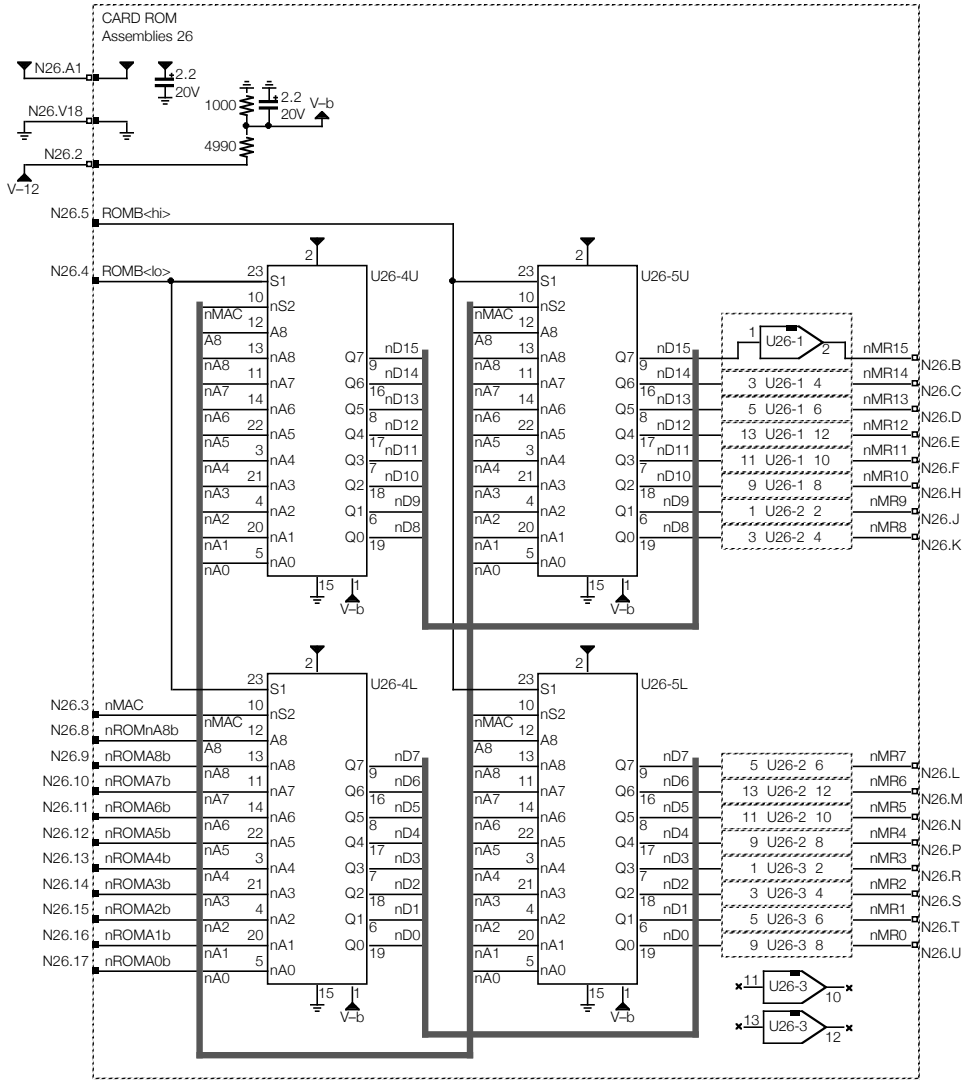
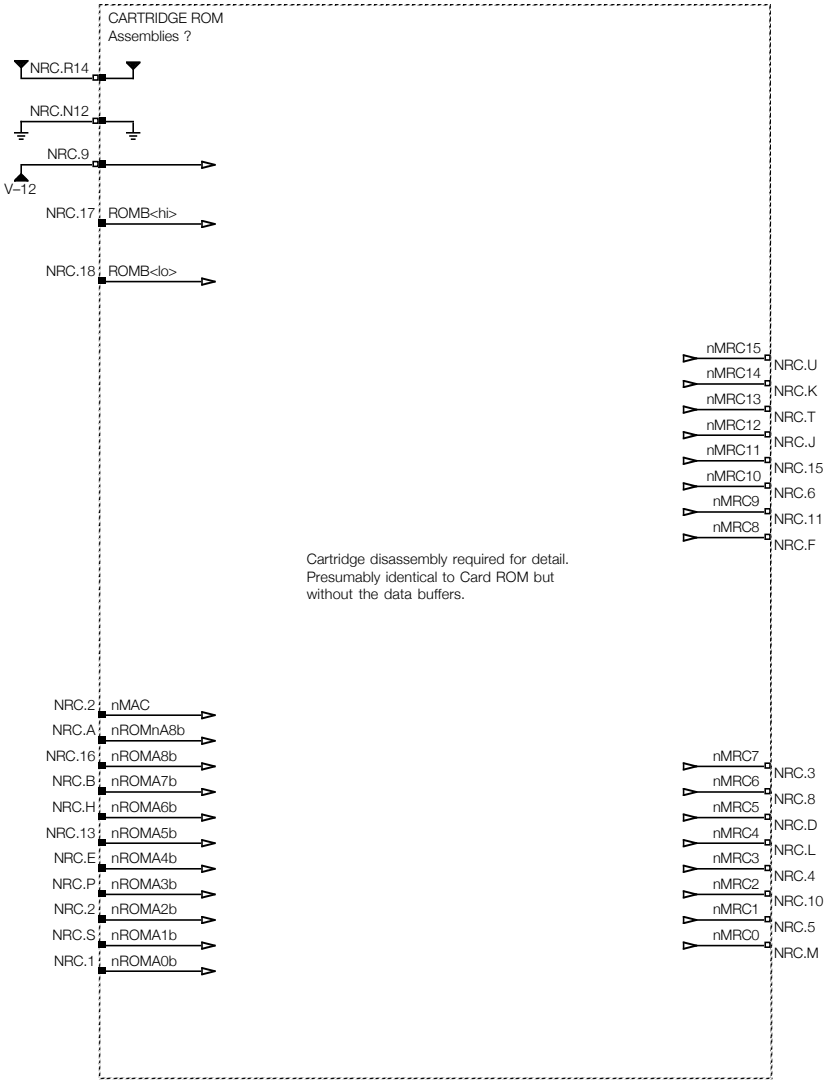
Section: Basic ROM

Page: M5 Rendition: 2014 Dec 26





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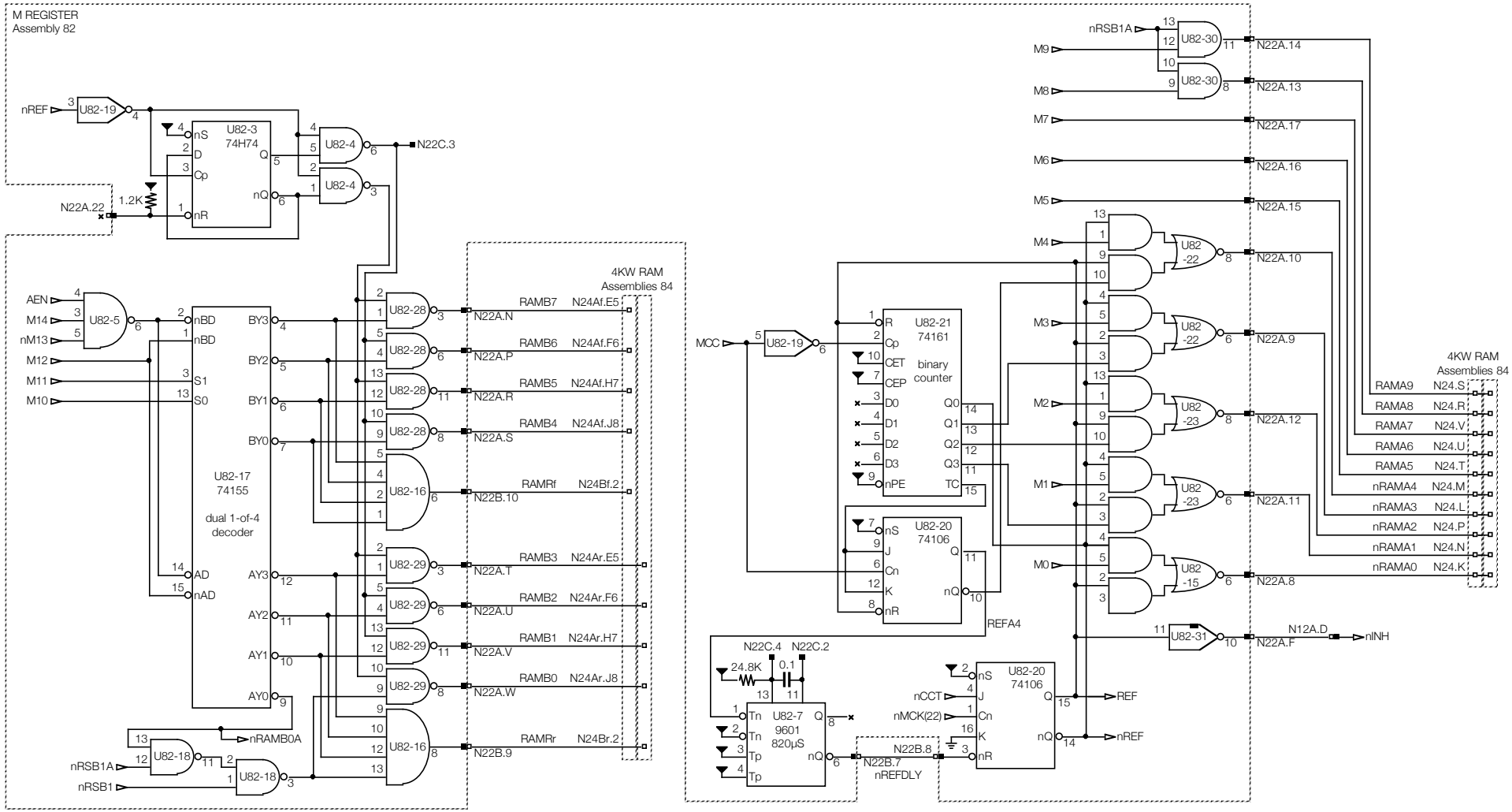
Section: ROM Cards & Cartridges

Page: M6 Rendition: 2014 Dec 26



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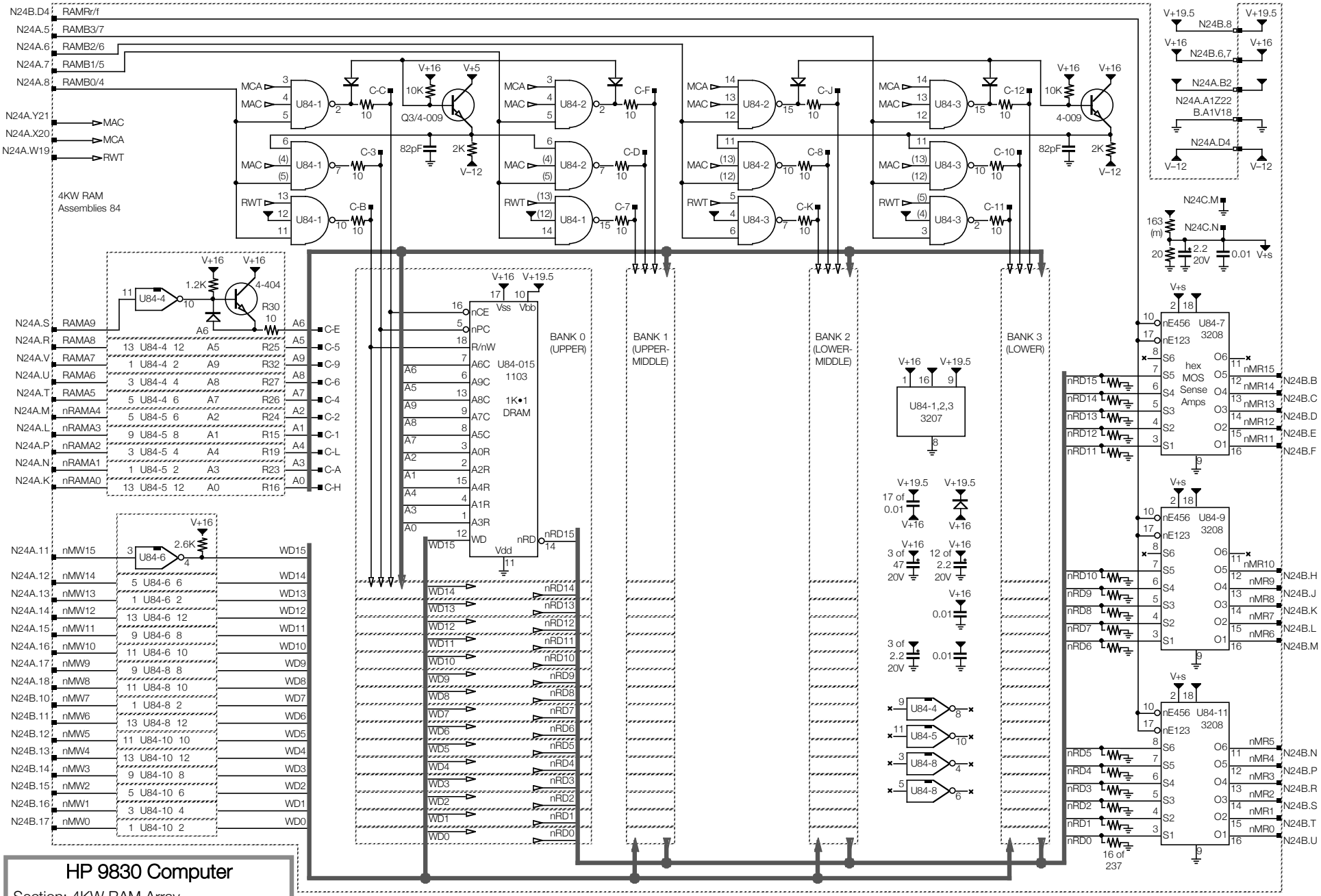
Section: RAM Addressing

Page: M7 Rendition: 2014 Dec 26



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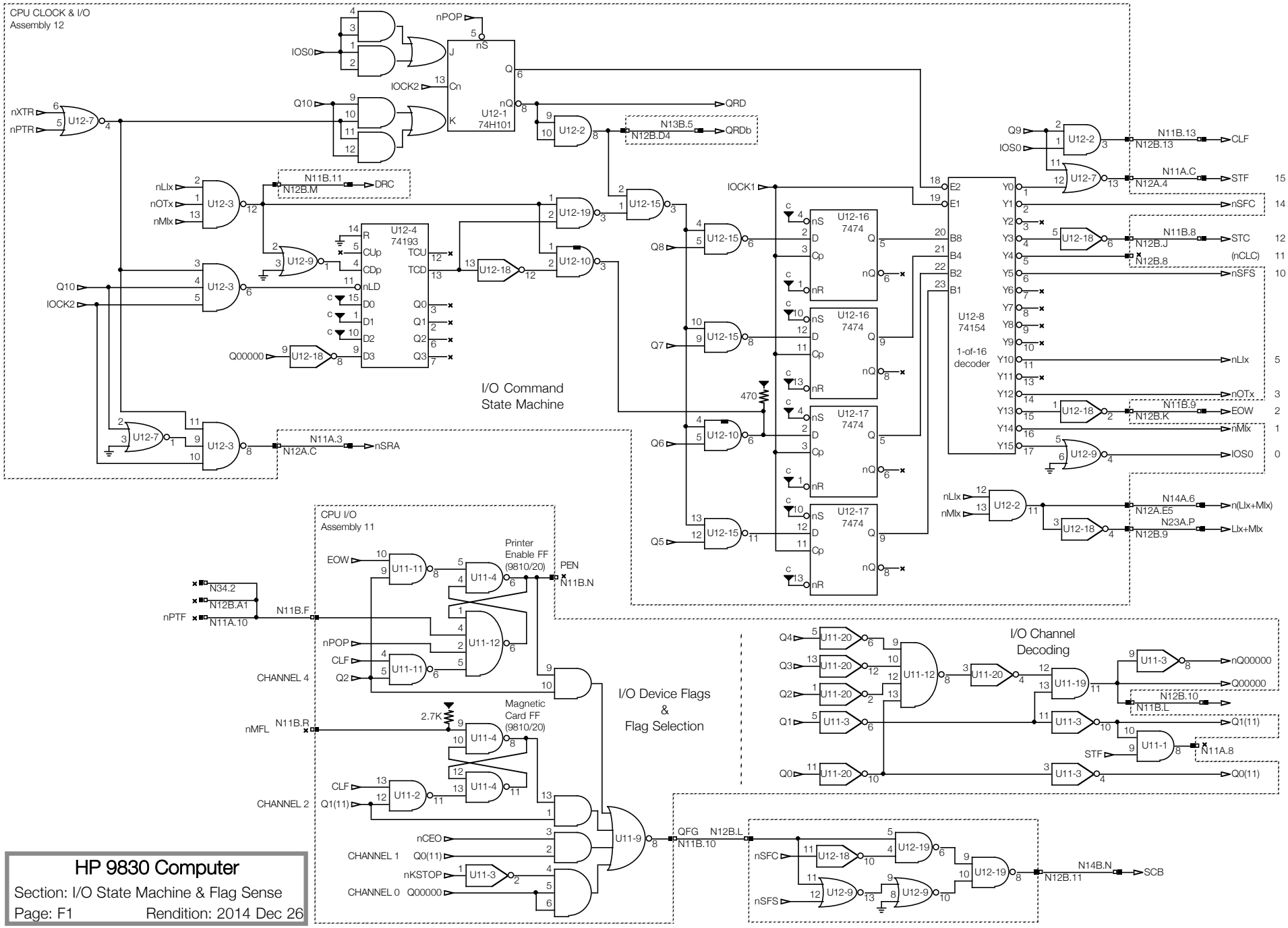
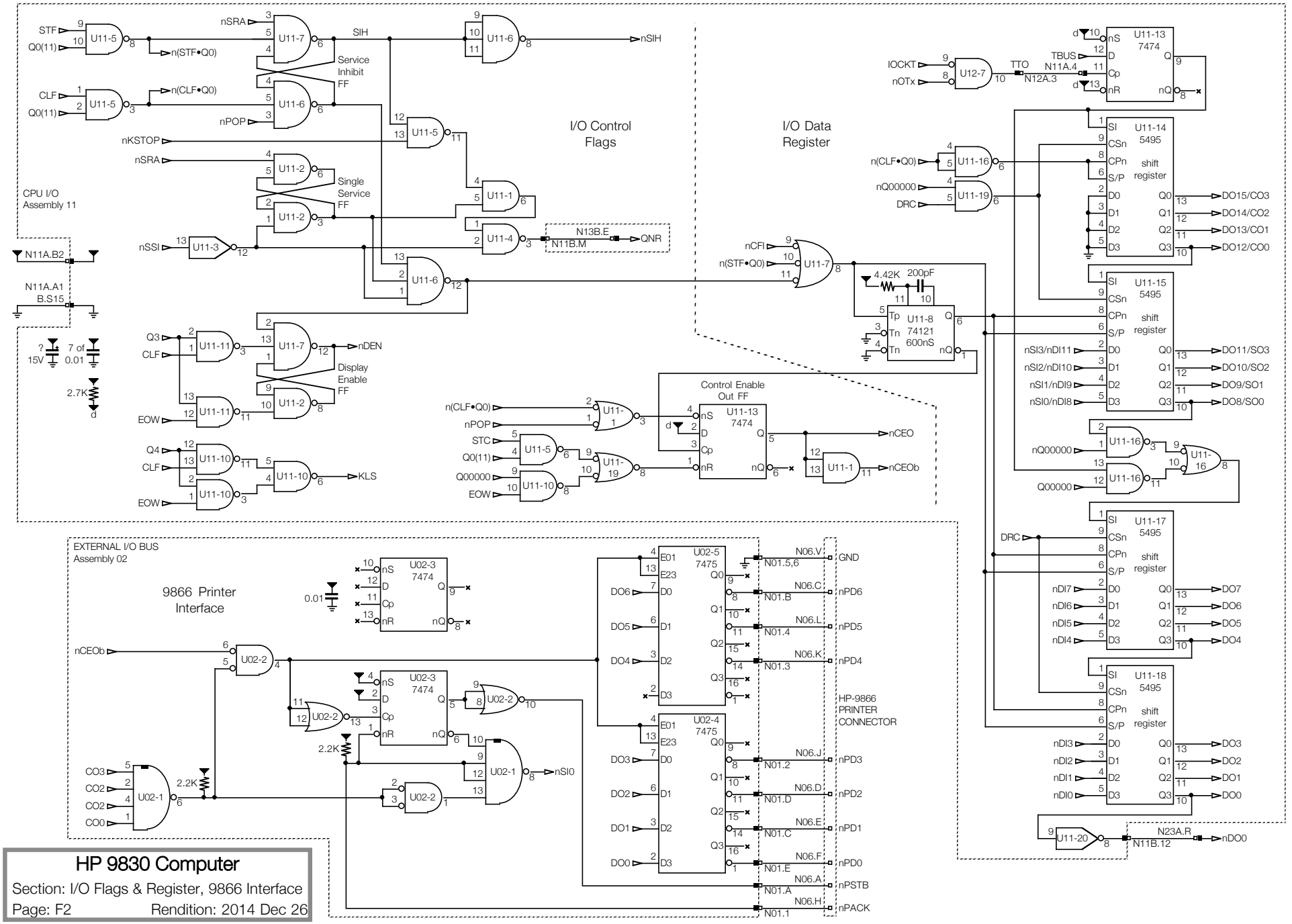
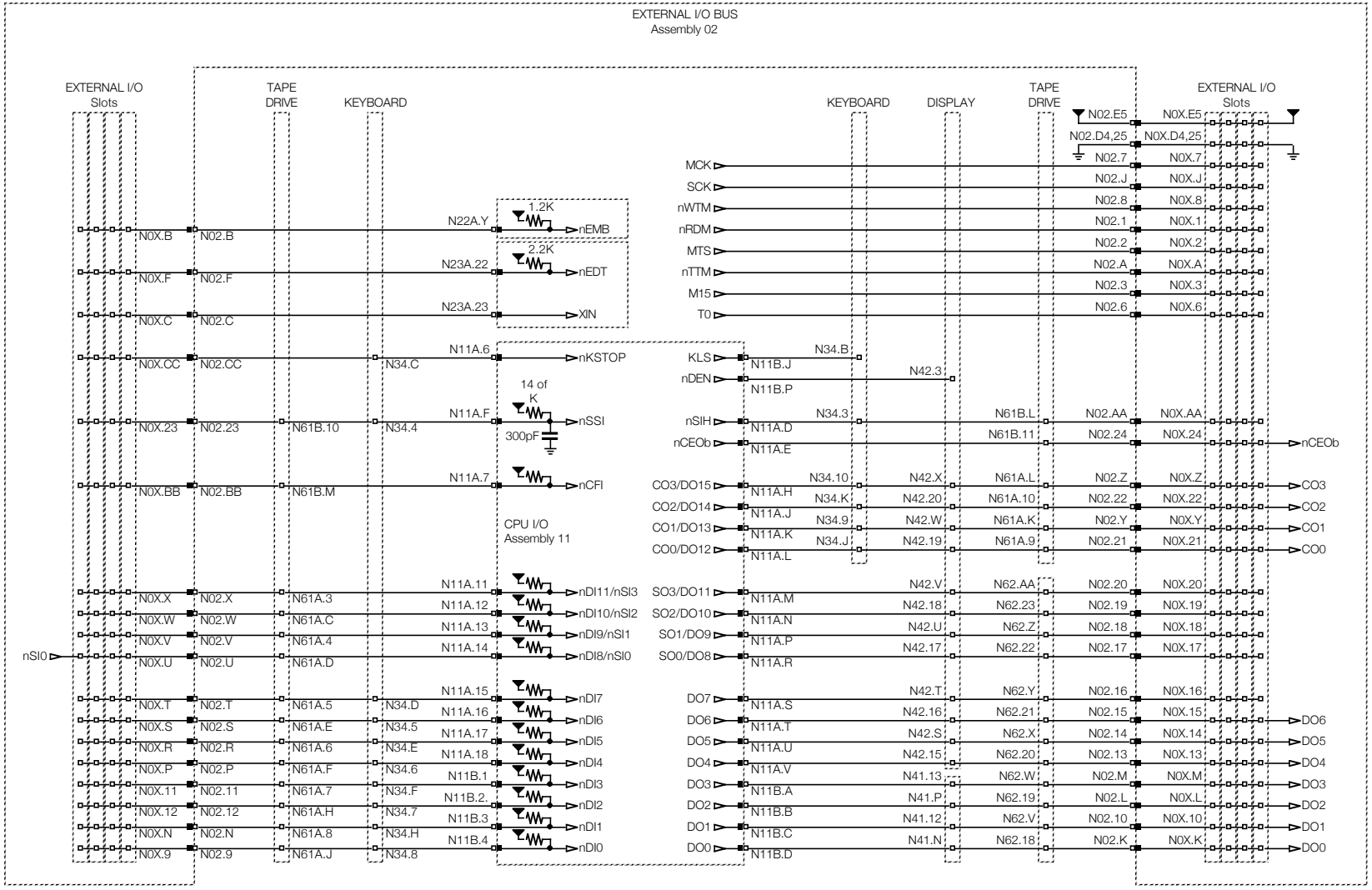
Section: 4KW RAM Array

Page: M8 Rendition: 2014 Dec 26


CPU CLOCK & I/O
Assembly 12
I/O Command
State Machine
U12-1
74H101
U12-4
74193
U12-8
74154
1-of-16
decoder
U12-16
7474
U12-17
7474
CPU I/O
Assembly 11
Printer
Enable FF
(9810/20)
Magnetic
Card FF
(9810/20)
I/O Device Flags
&
Flag Selection
I/O Channel
Decoding
HP 9830 Computer
Section: I/O State Machine & Flag Sense
Page: F1
Rendition: 2014 Dec 26


CPU I/O
Assembly 11
I/O Control
Flags
I/O Data
Register
Service
Inhibit
FF
Single
Service
FF
Display
Enable
FF
Control Enable
Out FF
shift
register
EXTERNAL I/O BUS
Assembly 02
9866 Printer
Interface
HP-9866
PRINTER
CONNECTOR
HP 9830 Computer
Section: I/O Flags & Register, 9866 Interface
Page: F2
Rendition: 2014 Dec 26



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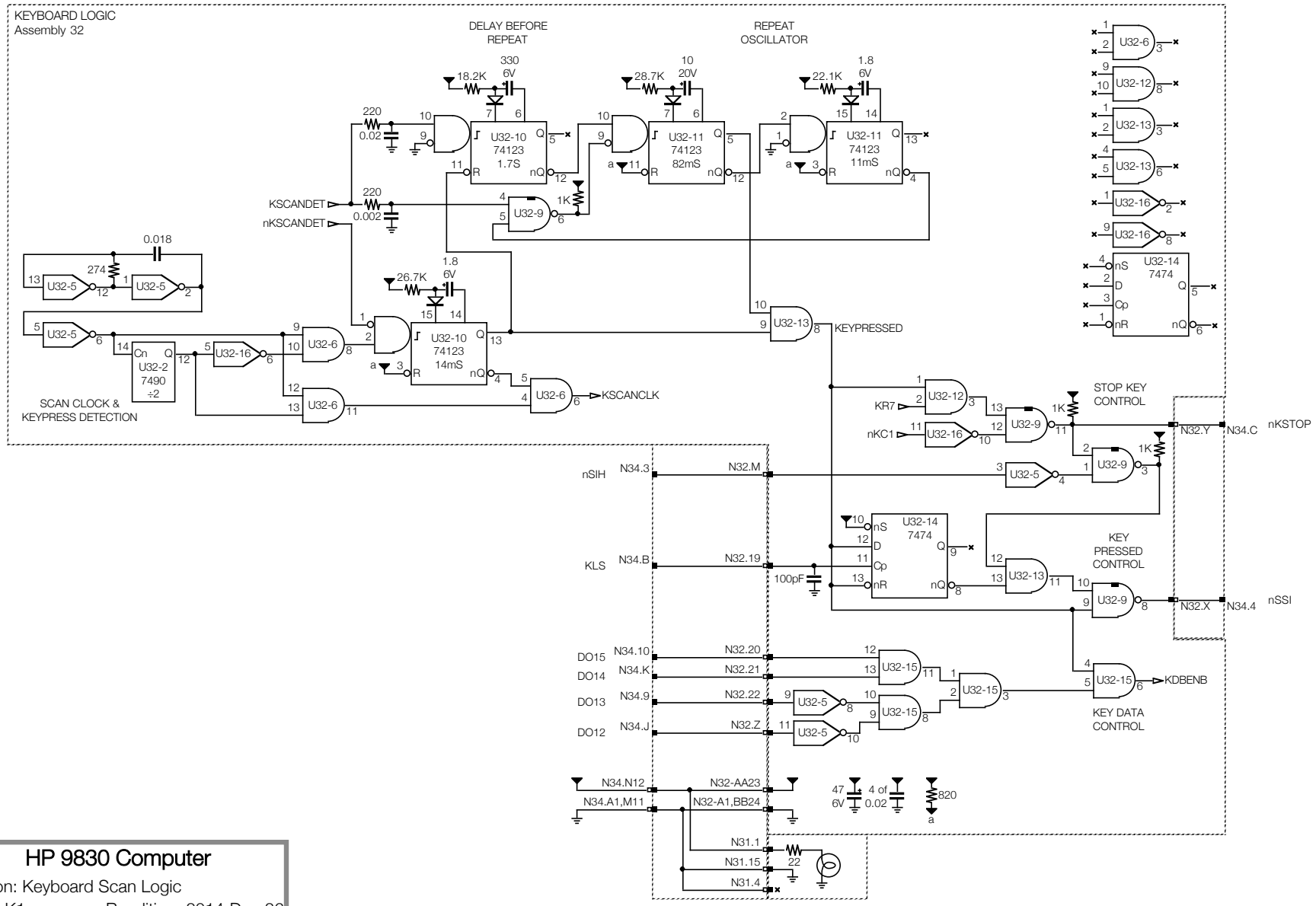
Section: I/O Busses

Page: F3 Rendition: 2014 Dec 26



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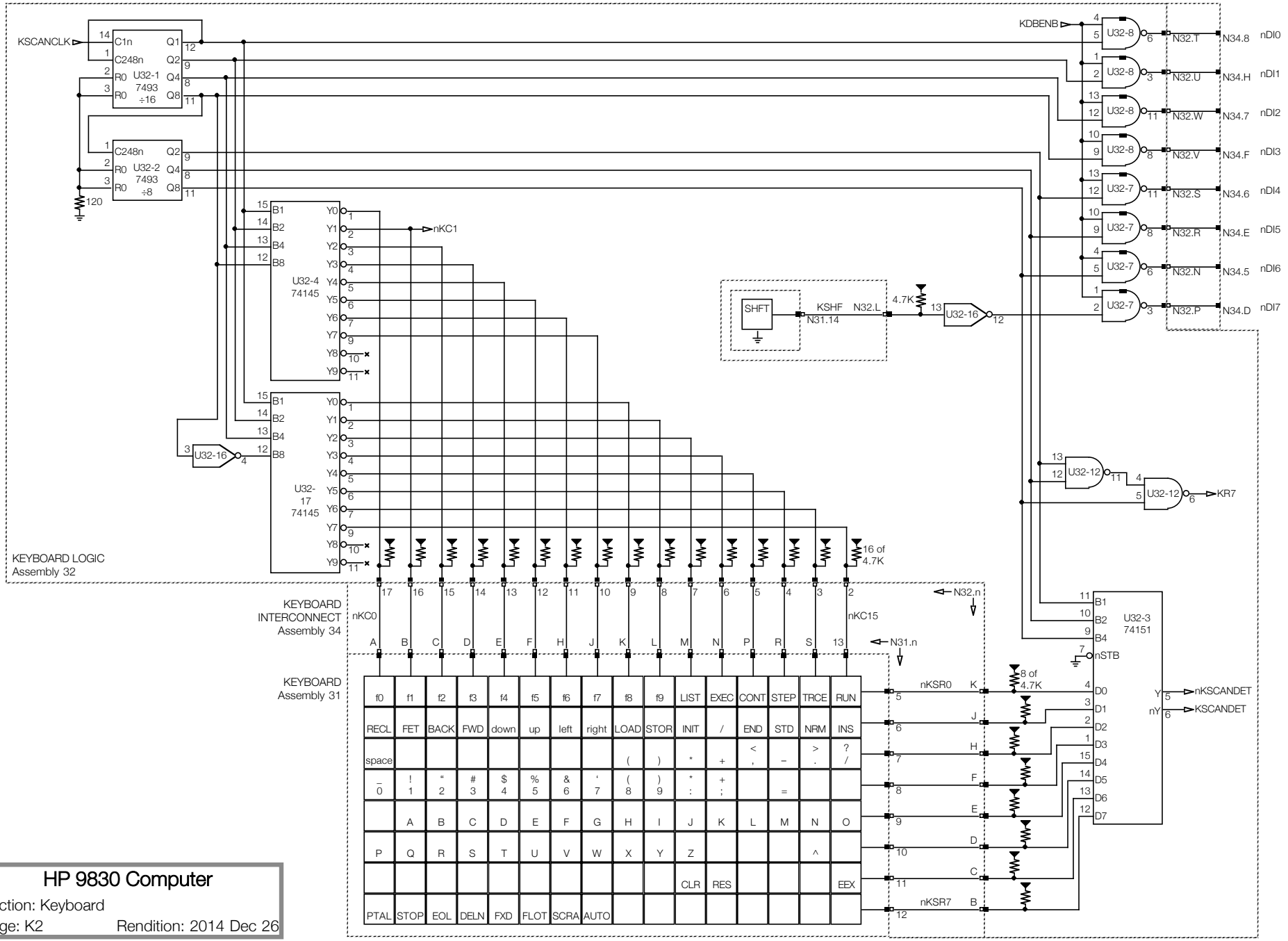
Section: Keyboard Scan Logic

Page: K1 Rendition: 2014 Dec 26



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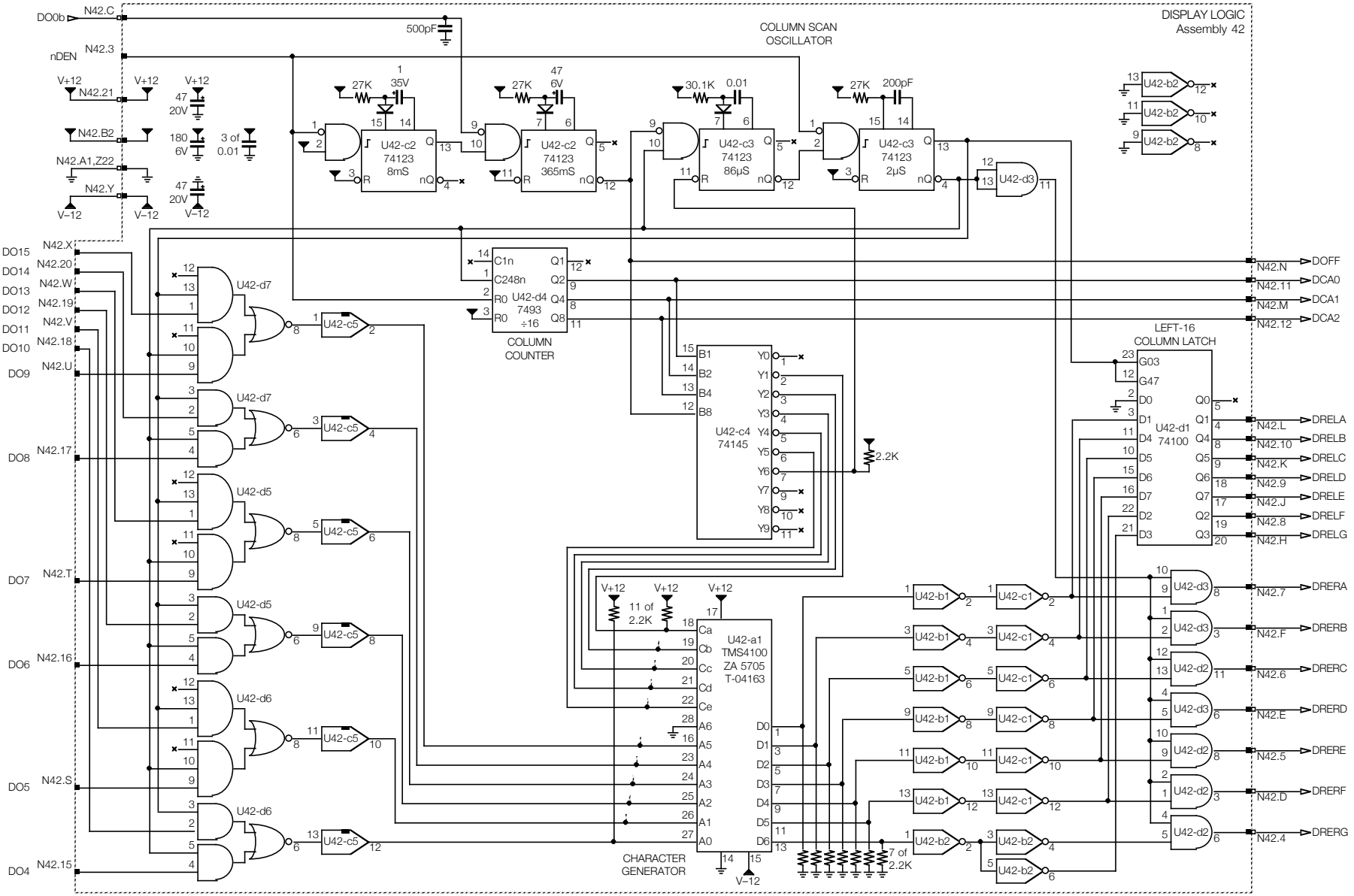
Section: Keyboard

Page: K2 Rendition: 2014 Dec 26



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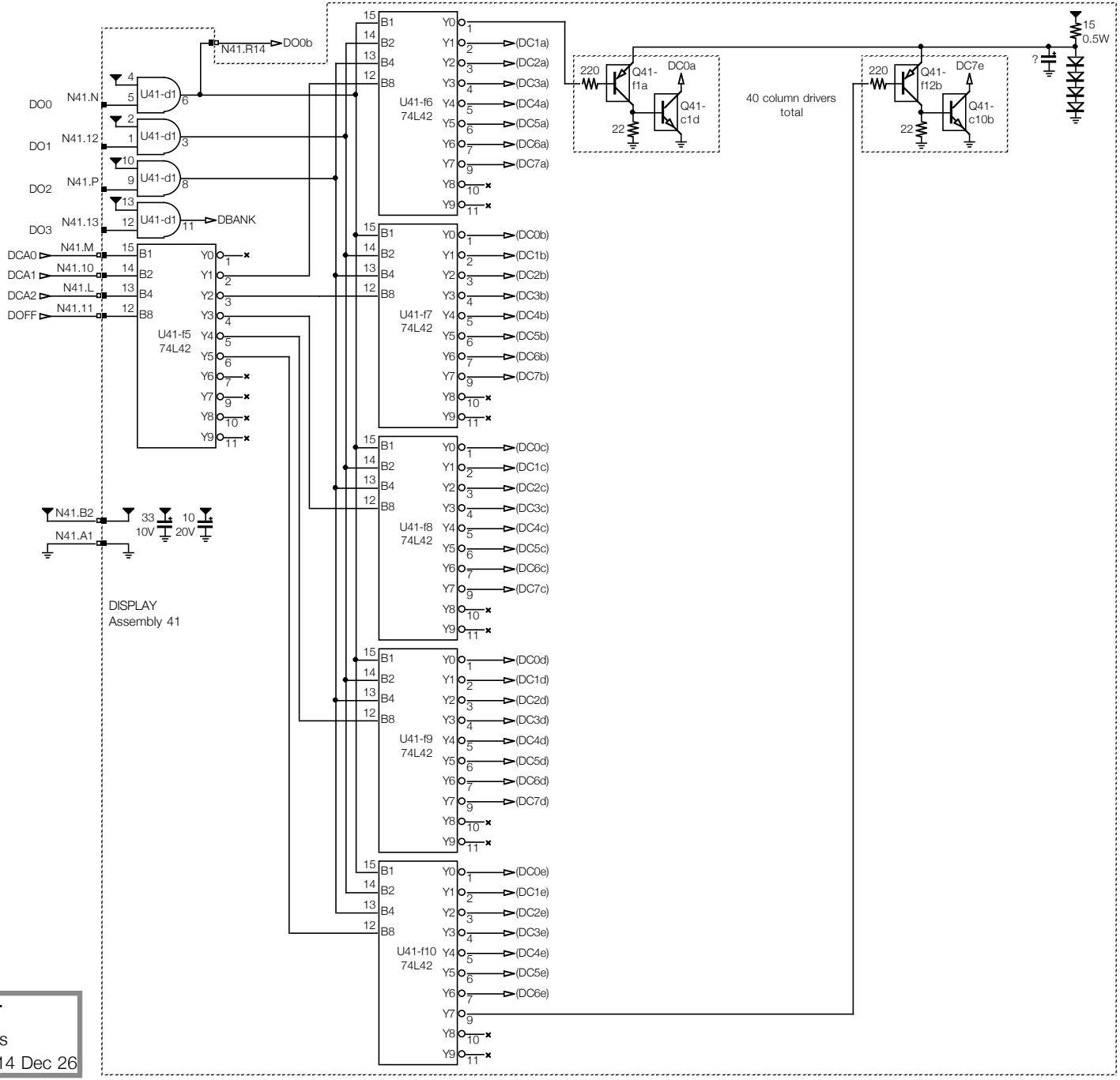
Section: Display Logic

Page: D1 Rendition: 2014 Dec 26



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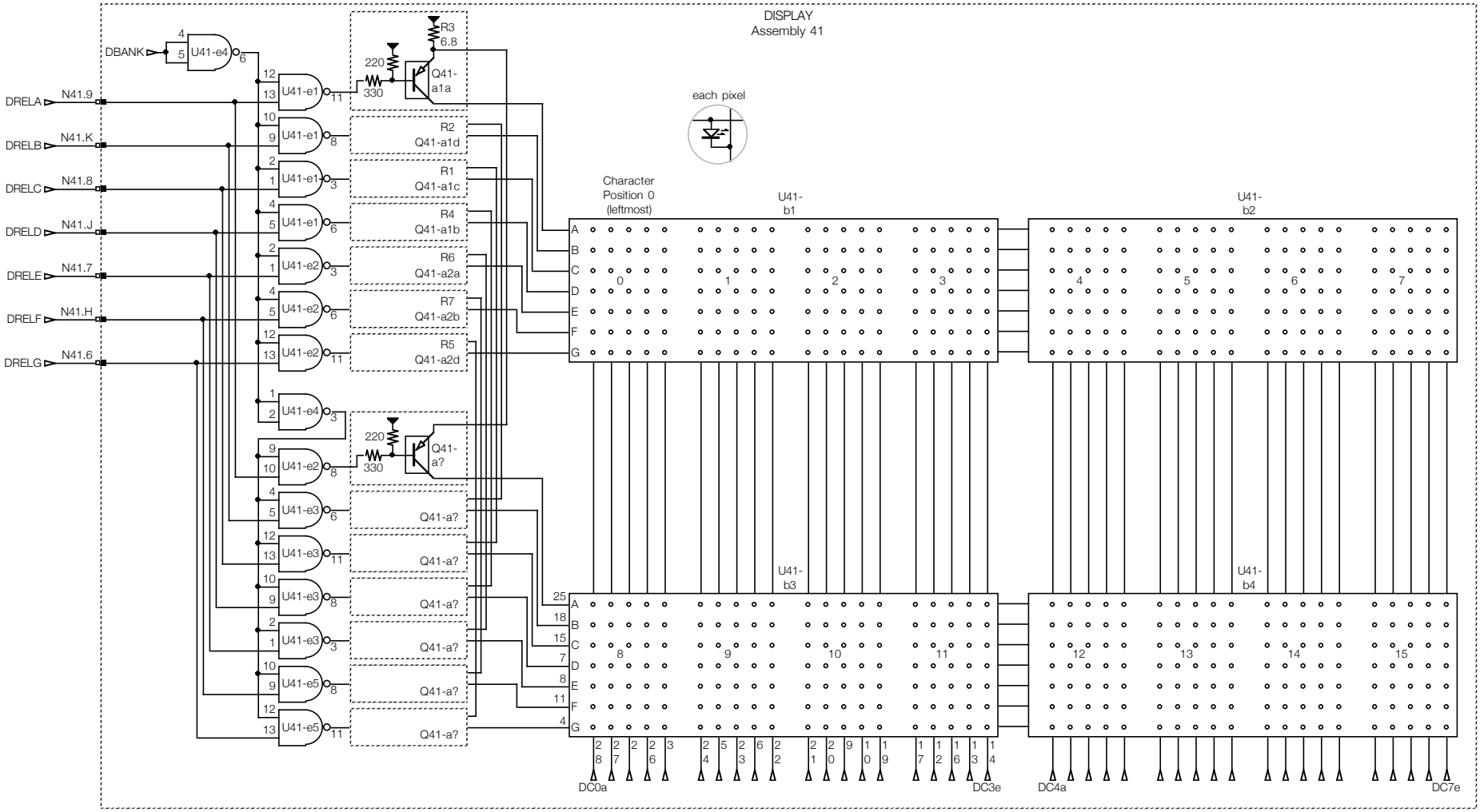
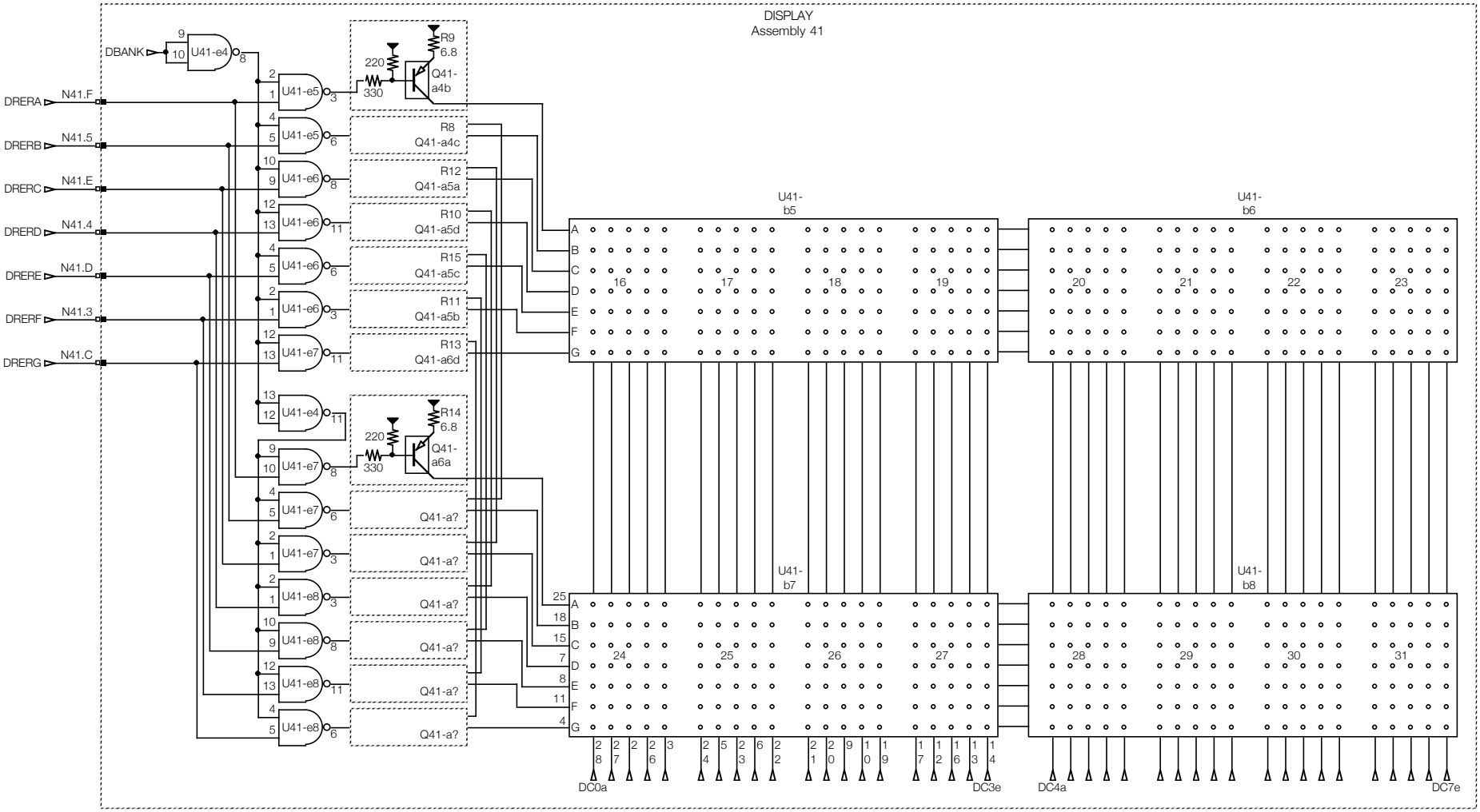
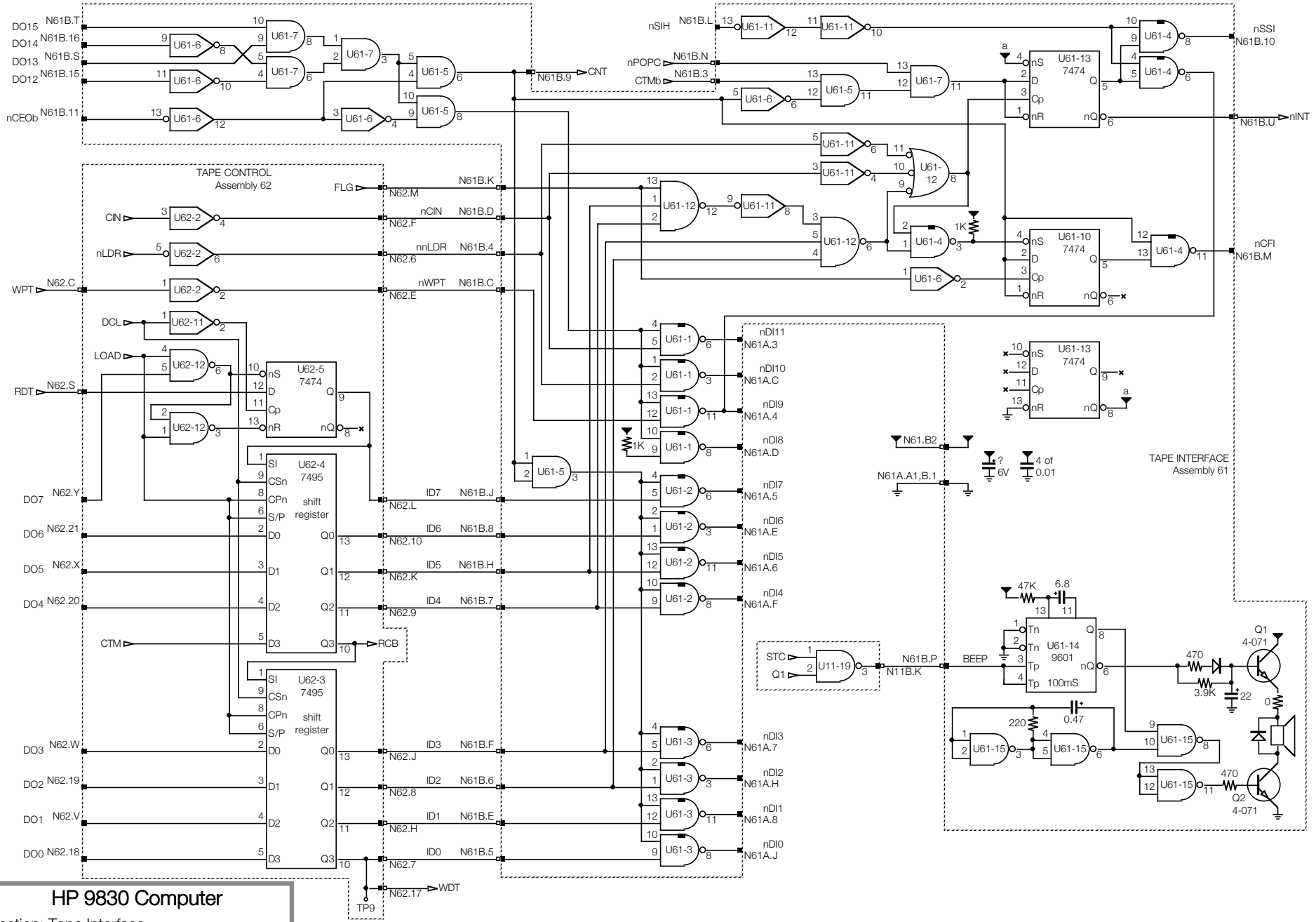
Section: Display Column Decoders

Page: D2 Rendition: 2014 Dec 26


DISPLAY
Assembly 41
each pixel
DBANK
DRELA
DRELB
DRELC
DRELD
DRELE
DRELF
DRELG
N41.9
N41.K
N41.8
N41.J
N41.7
N41.H
N41.6
U41-e4
U41-e1
U41-e2
U41-e3
U41-e5
R3
6.8
220
330
Q41-a1a
R2
Q41-a1d
R1
Q41-a1c
R4
Q41-a1b
R6
Q41-a2a
R7
Q41-a2b
R5
Q41-a2d
Q41-a?
Character
Position 0
(leftmost)
U41-b1
U41-b2
U41-b3
U41-b4
A
B
C
D
E
F
G
DC0a
DC3e
DC4a
DC7e


DISPLAY
Assembly 41
DBANK
U41-e4
DRERA
DRERB
DRERC
DRERD
DRERE
DRERF
DRERG
N41.F
N41.5
N41.E
N41.4
N41.D
N41.3
N41.C
U41-e5
U41-e6
U41-e7
U41-e8
R9 6.8
R8
R12
R10
R15
R11
R13
R14 6.8
220
330
Q41-a4b
Q41-a4c
Q41-a5a
Q41-a5d
Q41-a5c
Q41-a5b
Q41-a6d
Q41-a6a
Q41-a?
U41-b5
U41-b6
U41-b7
U41-b8
A
B
C
D
E
F
G
DC0a
DC3e
DC4a
DC7e



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Section: Tape Interface

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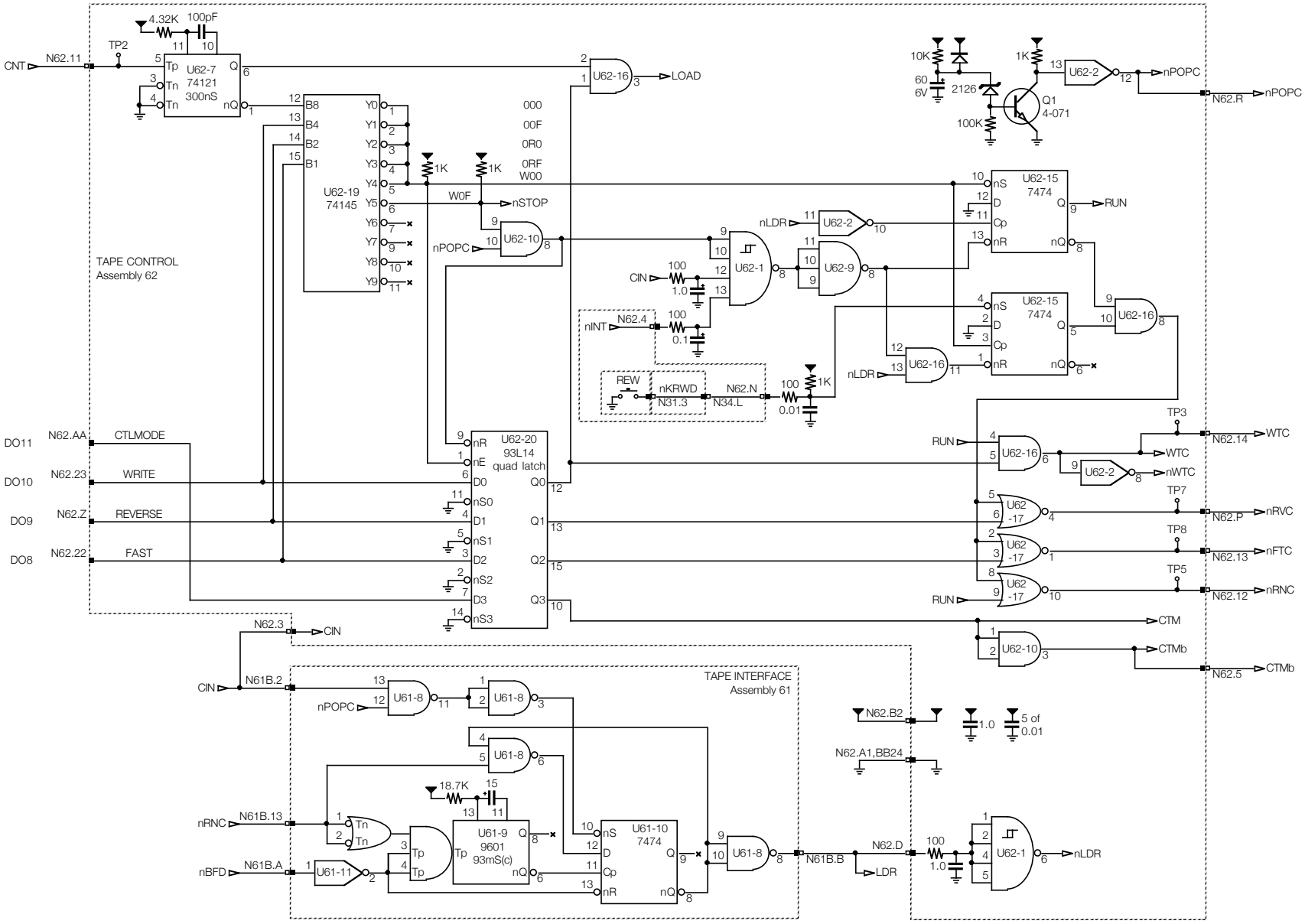

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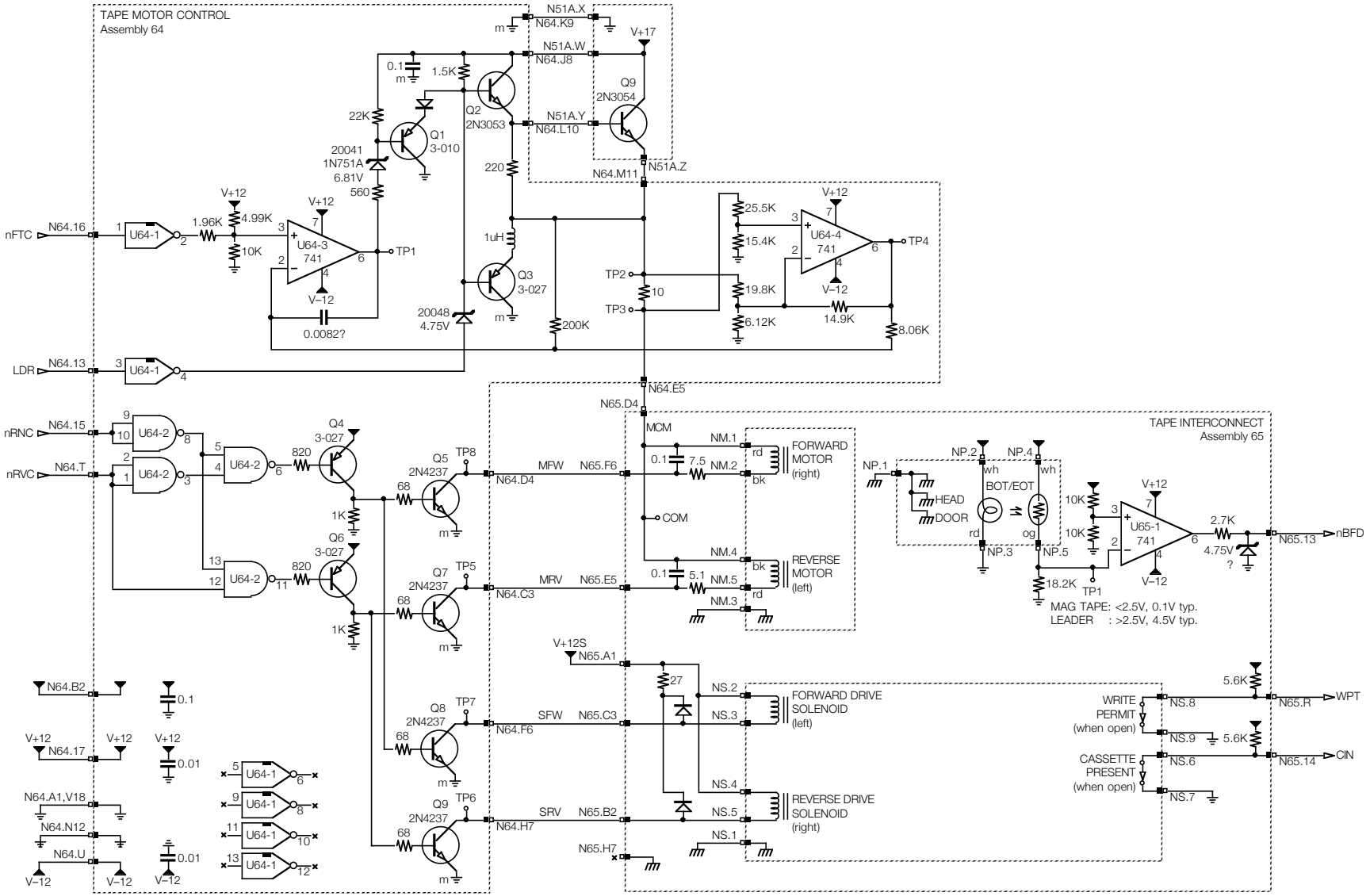
Section: Tape Command Decode

Page: T2 Rendition: 2014 Dec 26



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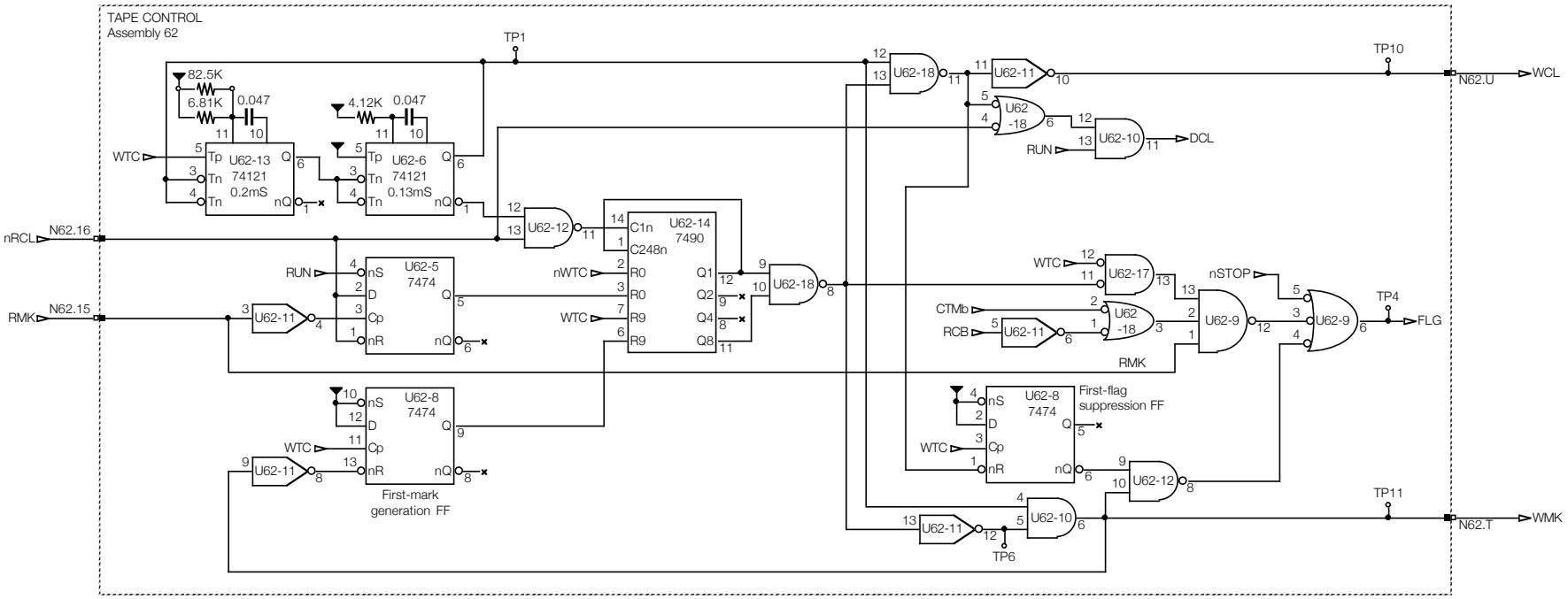
Section: Tape Drive

Page: T3 Rendition: 2014 Dec 26



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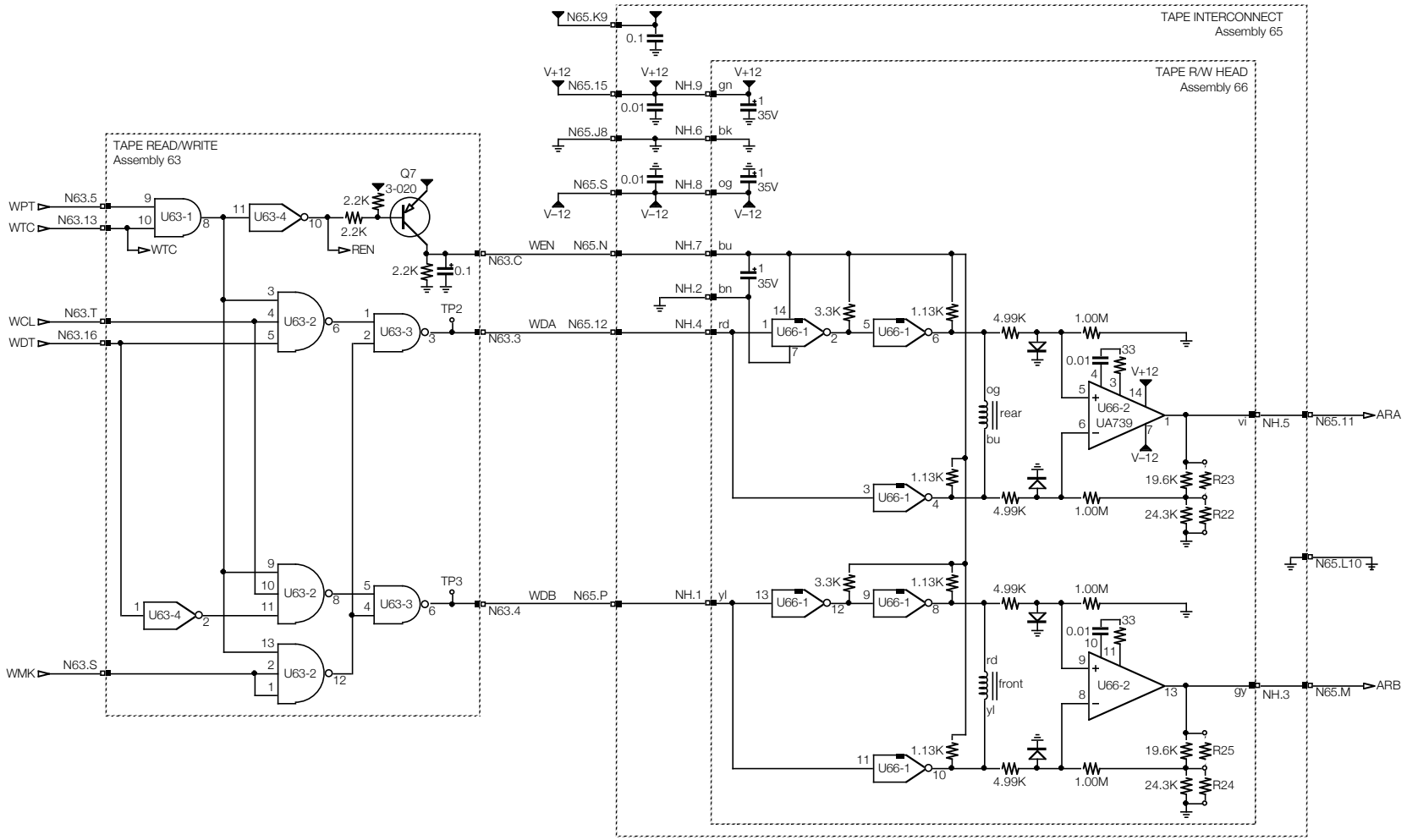
Section: Tape Data Clock

Page: T4 Rendition: 2014 Dec 26



	R22	R24
9830:	28.7K	28.7K
9865-0869:	24.3K	26.1K
9865-1570:	15.8K	15.8K

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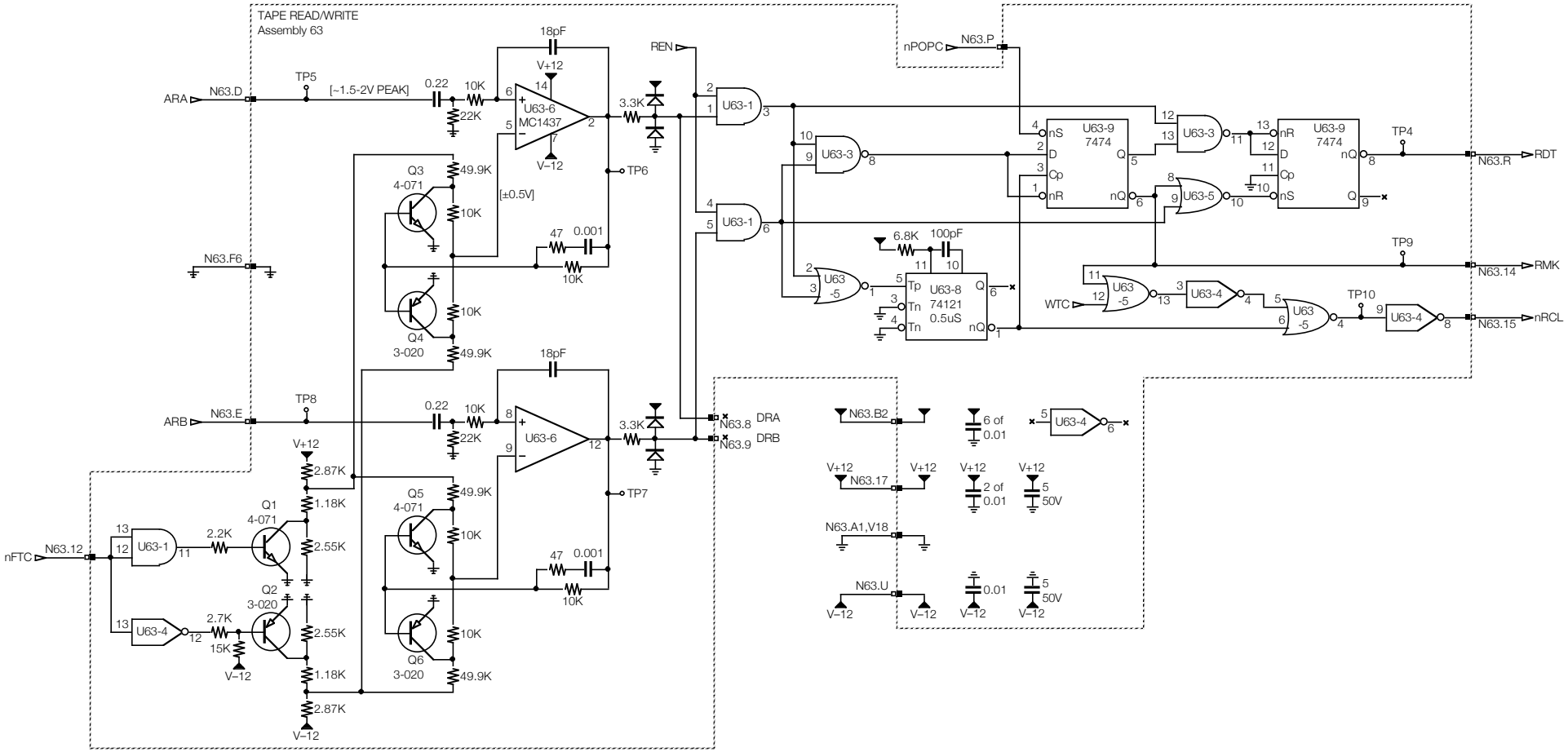
Section: Tape Read/Write

Page: T5 Rendition: 2014 Dec 26



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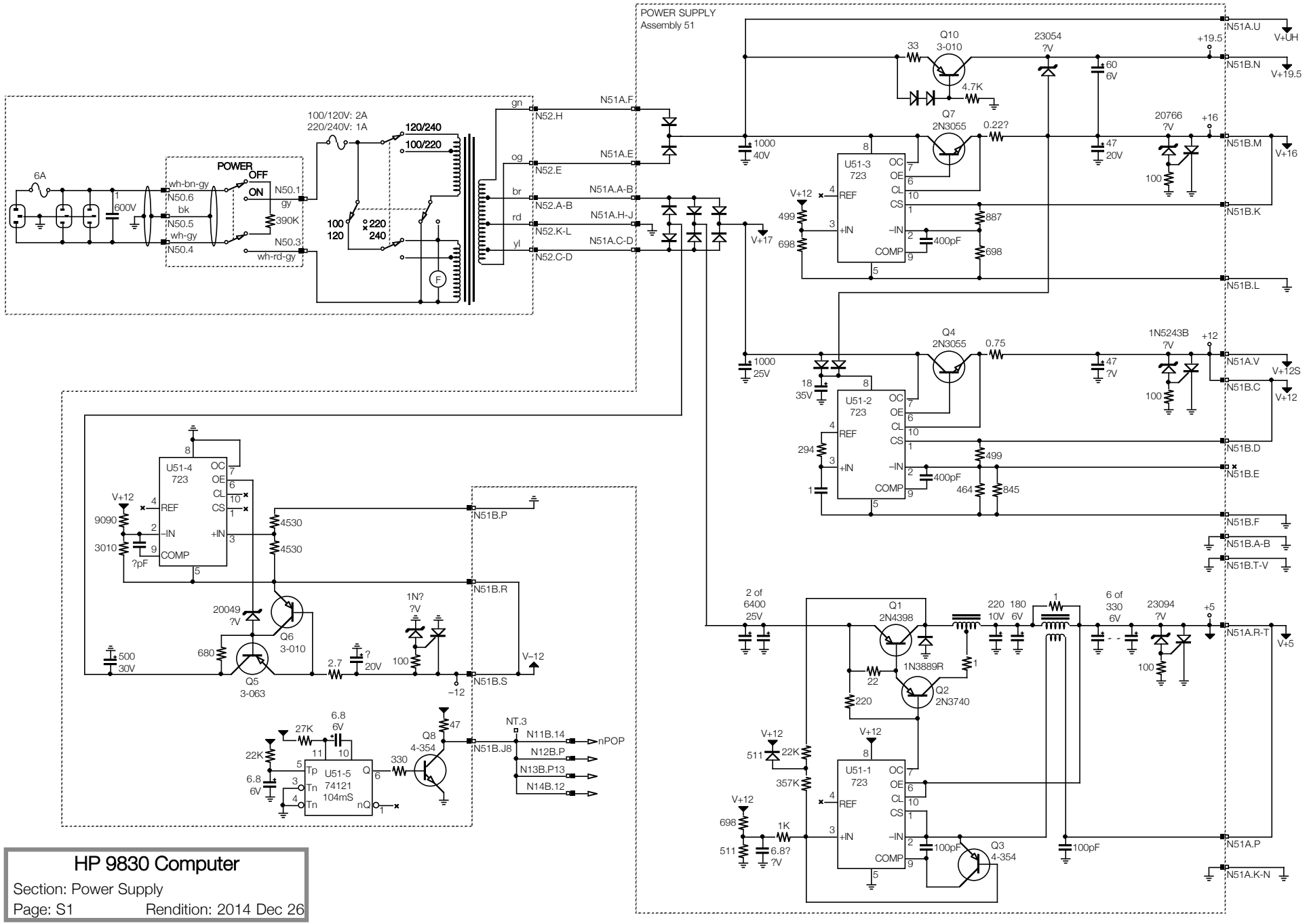
Section: Tape Read

Page: T6 Rendition: 2014 Dec 26



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Section: Power Supply

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IC Units

IC	Type	IC	Type	IC	Type	IC	Type	IC	Type	IC	Type	IC	Type	IC	Type
U02-1	74H22	U13-1	7404	U21-1	7416	U83-1	7402	U32-1	7493	U41-a1	(NPN)	U42-a1	TMS4100	U62-1	7413
	MC3012	U13-2	74H101	U21-2	7416	U83-2	74H52	U32-2	7493	U41-a2	(NPN)	U42-b1	74L04	U62-2	7404
U02-2	7402	U13-3	5495	U21-3	7416	U83-3	7495	U32-3	74151	U41-a3	(NPN)	U42-b2	74L04	U62-3	7495
U02-3	7474	U13-4	74H10	U21-4	7417	U83-4	7495	U32-4	74145	U41-a4	(NPN)	U42-c1	7404	U62-4	7495
U02-4	7475	U13-5	74150	U21-5	7417	U83-5	7495	U32-5	74S04	U41-a5	(NPN)	U42-c2	74123	U62-5	7474
U02-5	7475	U13-6	3601	U21-6	7417	U83-6	7495	U32-6	7408	U41-a6	(NPN)	U42-c3	74123	U62-6	74121
		U13-7	3601	U21-7	7417	U83-7	74H00	U32-7	7403	U41-a7	(NPN)	U42-c4	74145	U62-7	74121
U03-11	7417	U13-8	74H108	U21-8	7417	U83-8	74H54	U32-8	7403	U41-b1	(5*7 LED)	U42-c5	7407	U62-8	7474
U03-12	7417	U13-9	74H108	U21-9	7417	U83-9	74H08	U32-9	7403	U41-b2	(5*7 LED)	U42-d1	74100	U62-9	7410
U03-13	7417	U13-10	74155	U21-10	7417		MC3001	U32-10	74123	U41-b3	(5*7 LED)	U42-d2	7408	U62-10	7408
		U13-11	74H08	ROMS	(HP ROM)	U83-10	7404	U32-11	74123	U41-b4	(5*7 LED)	U42-d3	7408	U62-11	7404
U11-1	7408	U13-12	5495			U83-11	7404	U32-12	7408	U41-b5	(5*7 LED)	U42-d4	7493	U62-12	7400
U11-2	7400	U13-13	5495	U82-1	74106	U83-12	7404	U32-13	7408	U41-b6	(5*7 LED)	U42-d5	7451	U62-13	74121
U11-3	7404	U13-14	5495	U82-2	74H106	U83-13	7404	U32-14	7474	U41-b7	(5*7 LED)	U42-d6	7451	U62-14	7490
U11-4	7400	U13-15	9322	U82-3	74H74	U83-14	7404	U32-15	7408	U41-b8	(5*7 LED)	U42-d7	7451	U62-15	7474
U11-5	7400	U13-16	74H108	U82-4	74H00	U83-15	7404	U32-16	7404	U41-c1	(PNP)			U62-16	7408
U11-6	7410	U13-17	74H108	U82-5	7410			U32-17	74145	U41-c2	(PNP)	U51-1	723	U62-17	7402
U11-7	7410	U13-18	74155	U82-6	7432	U84-1	3207			U41-c3	(PNP)	U51-2	723	U62-18	7400
U11-8	74121	U13-19	3301A	U82-7	9601	U84-2	3207			U41-c4	(PNP)	U51-3	723	U62-19	74145
U11-9	7453	U13-20	3301A	U82-8	7495	U84-3	3207			U41-c5	(PNP)	U51-4	723	U62-20	93L14
U11-10	7400	U13-21	3301A	U82-9	7495	U84-4	7406			U41-c6	(PNP)	U51-5	74121		
U11-11	7400	U13-22	3301A	U82-10	7495	U84-5	7406			U41-c7	(PNP)			U63-1	7408
U11-12	7420	U13-23	3601	U82-11	7495	U84-6	7406			U41-c8	(PNP)	U61-1	7403	U63-2	7410
U11-13	7474			U82-12	7408	U84-7	3208			U41-c9	(PNP)	U61-2	7403	U63-3	7400
U11-14	5495	U14-1	5495	U82-13	7400	U84-8	7406			U41-c10	(PNP)	U61-3	7403	U63-4	7404
U11-15	5495	U14-2	74H62	U82-14	74H11	U84-9	3208			U41-d1	7408	U61-4	7403	U63-5	7402
U11-16	7400	U14-3	74H53	U82-15	74H51	U84-10	7406			U41-e1	7400	U61-5	7408	U63-6	MC1437
U11-17	5495	U14-4	5495	U82-16	74H21	U84-11	3208			U41-e2	7400	U61-6	7404	U63-8	74121
U11-18	5495	U14-5	5495	U82-17	74155	RAMS	1103			U41-e3	7400	U61-7	7408	U63-9	7474
U11-19	7408	U14-6	7491	U82-18	7400					U41-e4	7400	U61-8	7400		
U11-20	7404	U14-7	74H00	U82-19	7404	U25-1	7417			U41-e5	7400	U61-9	9601	U64-1	7406
		U14-8	74H08	U82-20	74H106	U25-2	7417			U41-e6	7400	U61-10	7474	U64-2	MC846
U12-1	74H10	U14-9	9328	U82-21	74161	U25-3	7416			U41-e7	7400	U61-11	7404	U64-3	741
U12-2	7408	U14-10	9328	U82-22	74H51	U25-4	7416			U41-e8	7400	U61-12	7410	U64-4	741
U12-3	7410	U14-11	3601	U82-23	74H51	U25-5	7416			U41-e9	(NPN)	U61-13	7474		
U12-4	74193	U14-12	7474	U82-24	7437	U25-6	74154			U41-e10	(NPN)	U61-14	9601	U65-1	741
U12-5	74H00	U14-13	74H00	U82-25	7400					U41-e11	(NPN)	U61-15	7400		
U12-6	74H74	U14-14	74H21	U82-26	74H04	U26-1	7417			U41-e12	(NPN)			U66-1	7406
U12-7	7402	U14-15	7432	U82-27	7408	U26-2	7417			U41-f1	(NPN)			U66-2	UA739
U12-8	74154	U14-16	N8885A	U82-28	7400	U26-3	7417			U41-f2	(NPN)				
U12-9	7402	U14-17	74H00	U82-29	7400	ROMS	(HP ROM)			U41-f3	(NPN)				
U12-10	7403	U14-18	74H00	U82-30	7408					U41-f4	(NPN)				
U12-11	74H00	U14-19	3601	U82-31	7416					U41-f5	74L42				
U12-12	74H20	U14-20	74H01	U82-32	74154					U41-f6	74L42				
U12-13	74H40			U82-33	7400					U41-f7	74L42				
U12-14	74193			U82-34	7400					U41-f8	74L42				
U12-15	7400									U41-f9	74L42				
U12-16	7474									U41-f10	74L42				
U12-17	7474									U41-f11	(NPN)				
U12-18	7404									U41-f12	(NPN)				
U12-19	7400														

Count: 306
Req. ROMS: 30

IC	Type	
BASIC I ROM		
U21-0L	1818-2064E	
U21-0U	1818-2065E	
U21-1L	1818-2066E	
U21-1U	1818-2067E	
U21-2L	1818-2190A	
U21-2U	1818-2191A	
U21-3L	1818-2070E	
U21-3U	1818-2071E	
U21-4L	1818-2072E	
U21-4U	1818-2073E	
U21-5L	1818-2074E	
U21-5U	1818-2075E	
U21-6L	1818-2194A	
U21-6U	1818-2077E	
U21-7L	1818-2078E	
U21-7U	1818-2079E	
U21-10L	1818-2080E	
U21-10U	1818-2081E	
U21-11L	1818-2082E	
U21-11U	1818-2083E	
U21-12L	1818-2084E	
U21-12U	1818-2085E	
U21-13L	1818-2086E	
U21-13U	1818-2087E	
U21-14L	1818-2182A	
U21-14U	1818-2183A	
U21-15L	1818-2184A	
U21-15U	1818-2185A	
BASIC II Card ROM		
	09830-66526	
U26-4L	1818-?	
U26-4U	1818-?	
U26-5L	-	
U26-5U	-	
String Variables Card ROM		
	11274-66520	
U26-4L	1818-2186A	B-636D
U26-4U	1818-2187A	B-675B
U26-5L	1818-2188A	B-656B
U26-5U	1818-2189A	B-741C
Plotter Card ROM		
	11271-66520	
U26-4L	1818-2116B	B-805B
U26-4U	1818-2117B	C-033D
U26-5L	1818-2118B	C-071A
U26-5U	1818-2119B	C-083A

IC Types & Power Pins

Type	HP #	V+	5 GND	Function	Qty.	Type	HP #	V+	5 GND	Function	Qty.
7400	1820-0054	14	7	NAND 2-in / quad	28	74100		24	7	4-bit latch / dual	1
74H00	1820-0370	14	7	"	8	74H101		14	7	FF JK	1
74H01	1820-0605	14	7	NAND 2-in OC / quad	1	74106		5	13	FF JK / dual	1
7402	1820-0328	14	7	NOR 2-in / quad	6	74H106		5	13	"	2
7403	1820-0269	14	7	NAND 2-in OC / quad	8	74H108		14	7	FF JK /dual	4
7404	1820-0174	14	7	NOT / hex	18	74121		14	7	monostable	6
74H04	1820-0424	14	7	"	1	74123		16	8	monostable /dual	4
74L04		14	7	"	2	74145		16	8	decoder 1-of-10 OC	4
74S04		14	7	"	1	74150		24	12	multiplexer 16-in	1
7406	1820-0471	14	7	NOT OC hi-V / hex	7	74151		16	8	multiplexer 8-in	1
7407		14	7	buffer OC hi-V / hex	1	74154	1820-0495	24	12	decoder 1-of-16	3
7408	1820-0511	14	7	AND 2-in / quad	18	74155		16	8	decoder 1-of-4 / dual	3
74H08		14	7	"	2	74161		16	8	counter 4-bit binary syncl	1
74H08/M	1820-0141	14	7	"	1	74193	1820-0233	16	8	counter 4-bit binary up/d	2
7410	1820-0068	14	7	NAND 3-in/ triple	7						
74H10	1820-0371	14	7	"	2	93L14	1820-0701	16	8	latch 4-bit	1
74H11		14	7	AND 3-in/ triple	1	9322	1820-0616	16	8	multiplexer 2-in / quad	1
7413	1820-0537	14	7	NAND 4-in schmitt /dual	1	9328	1820-0741	16	8	SR 8-bit /dual	2
7416	1820-0577	14	7	NOT OC hi-V buffer / hex	7	9601	1820-0207	14	7	monostable	3
7417	1820-0618	14	7	buffer OC hi-V / hex	15						
7420		14	7	NAND 4-in /dual	1	MC846	1820-0094	14	7	NAND 2-in DTL / quad	1
74H20		14	7	"	1	N8885A	1820-0923	14	7	NOR 2-in / quad	1
74H21	1820-0374	14	7	AND 4-in / dual	2						
74H22		14	7	NAND 4-in OC /dual	1	1103		*		RAM 1K*1	128
7432	1820-0661	14	7	OR 2-in / quad	2	3207		*		drivers for 1103s / quad	3
7437		14	7	NAND 2-in buffer / quad	1	3208		*		amps for 1103s / hex	3
74H40	1820-0376	14	7	NAND 4-in buffer / dual	1	3301A		16	8	ROM 256*4	4
74L42	1820-0777	16	8	decoder 1-of-10	6	3601		16	8	ROM 256*4	5
7451		14	7	AOI 2-2 / dual	3	(HP ROM)		*		ROM 512*8	30
74H51	1820-0378	14	7	"	3	TMS4100		*		ROM char. gen.	1
74H52		14	7	AO 2-2-2-3-e	1						
7453		14	7	AOI 2-2-2-2-e	1	(5*7 LED)	1990-0343	-		5*7 LED display / quad	8
74H53	1820-0380	14	7	AOI 2-2-2-3-e	1						
74H54		14	7	AOI 2-2-2-2	1	723	1820-0196	*		voltage regulator	4
74H62	1820-0385	14	7	AO expander 2-2-3-3	1	UA739	1826-0044	*		linear amp / dual	1
7474	1820-0077	14	7	FF D / dual	12	741	1820-0203	*		op amp	3
74H74	1820-0512	14	7	"	2	MC1437L	1826-0019	*		op amp / dual	1
7475	1820-0301	5	12	latch 4-bit	2						
7490		5	10	counter decade	1	(NPN)	1858-0014	-		transistors NPN / quad	17
7491	1820-0364	5	10	SR 8-bit	1	(PNP)	1858-0027	-		transistors PNP / quad	10
7493		5	10	counter 12	3						
7495	1820-0367	14	7	SR 4-bit	10						
5495		14	7	"	11						
43					203	34					261

Number of IC types: 77
Number of ICs: 464
Check: 464

* See circuit schematic for power connections

Monostable Pulse Time Calculations

IC	Type	C uF	R KOhm	t uS	t mS
U11-b4	74121	0.0002	4.42	0.613	
U82-7	9601	0.1	24.8	816	
U32-10	74123	330	18.2		1,746
U32-10		1.8	26.7		14
U32-11	74123	10	28.7		82
U32-11		1.8	22.1		11
U42-c2	74123	47	27		365
U42-c2		1	27		8
U42-c3	74123	0.01	30.1	86	
U42-c3	123 graph	0.0002	27	2	
U51-5	74121	6.8	22		104
U61-9	9601	15	18.7		93
U61-14	9601	6.8	47		104
U62-7	74121	0.0001	4.32	0.299	
U62-6	74121	0.047	4.12	134	
U62-13	74121	0.047	6	205	
U63-8	74121	0.0001	6.8	0.471	

Tape Head Amp Calculations

Divider U	19.6
Divider L	24.3
Divider L	16.8
Feedback R	1000
Series R	4.99
divider ratio	2.97
gain ratio	201.40
Gain	599
Output V (meas.)	1.5
Head V	0.0025

IC Notes

- 3301A microcode and 3601 ALU ROMS are pin-compatible with 74S387
  74S387: TI Memory Databook 1st Ed., 1975, pg 182.

CPU Clock

MCK	Master Clock \ 8MHz \ HPP: Memory Clock
SCK	Shift Clock \ basic bit-serial clock
RCK	ROM Clock \ defines one microcode cycle
nCCT	
nINH	Inhibit Clock \ OC line, normally used by memory system to stop processor during refresh. Single stepping control according to patent.
nIHC	Inhibit Clock \ turns off internal clock
XTC	External Clock
IOCK1	I/O Clock 1 \ for state machine
IOCK2	I/O Clock 2 \ for state machine
IOCKT	I/O Clock for transfer from T-bus

CPU Data

RBUS	ALU input
SBUS	ALU input
TBUS	ALU output
A<0..3>	A register outputs
B0	B register LSB
E0	E register LSB
P0	P register LSB (program counter)
Q<0..11>	Q register outputs (instruction register)
T<0..3>	T register outputs
BC	Binary Carry flag
DC	Decimal Carry flag

CPU Controls

POP	Power-On Pulse
MCDIS	Microcode DISable
nCCO	Control of shift Clock
nIPS	
CEM	
AC<0..2>	ALU function select
UTR	Unary to R-bus
PTR	P-reg to R-bus
QTR	Q-reg to R-bus
BCD	BCD ALU operation
XTR	A/B-reg to-R-bus
MTS	M-reg to S-bus
TTS	T-reg to S-bus
SC0	S-bus Selector bit 0
SC1	S-bus Selector bit 1

Memory

RDM	Read Memory
WTM	Write Memory
AEN	Address ENable
MEN	Memory ENable
REF	Refresh RAM
RWT	Read/WriTe to RAM
REFDLY	Refresh Delay
MCP	Memory Cycle state-machine flag
MCA	Memory Cycle state-machine flag
MCB	Memory Cycle state-machine flag
MCC	Memory Cycle state-machine flag
MAC	Memory ACcess
MTS	M register to S-bus
TTM	T-bus to M register
M<0..15>	M Register (Memory Address)
MR<0..15>	Memory Read bus
MRC<0..15>	Memory Read bus for Cartridges
MW<0..15>	Memory Write bus
ROMB<00..37>	ROM Bank select
ROMA<0..8>	ROM Address
ROMA<0..8>b	ROM Address buffered
RSB1	another version of ROM Bank Select
RAMA<0..9>	RAM Address Bits
RAMB<0..7>	RAM Bank select
RAMR<a,b>	RAM boaRd select
T<0..3>	T register outputs
TRI	T Register serial Input
TSC	T register Serial Clock
TPC	T register Parallel load Clock
TMC	T register Mode Control \ serial/parallel
EMB	Extended Memory Busy
MSTL	Memory Suppress T-register Load
EDT	External memory Data Transfer
XIN	External serial data IN

I/O

CO<0..3>	Device Select-Code Output Bus
SO<0..3>	State/Command Output Bus
DO<0..15>	Data Output Bus
SI<0..3>	Status Input Bus
DI<0..15>	Data Input Bus
CEO	Control Enable Output \ initiate I/O, enable device
SIH	Service Inhibit \ suppress interrupt
SSI	Service Request Strobe Input \ interrupt request
CFI	Channel Flag In \ ack/ready from device
SRA	Service Request Acknowledge \ interrupt ack
QNR	Not service r equest \ interrupt request
QRD	Qualifier ROM Disable \ disable proc during IO
QFG	Qualifier Flag \ for skip-flag instructions
SCB	Set Carry Bit
Q00000	5 LSBits of Q = 0 \ I/O channel 0
DRC	Data (IO) Register Clock
TTO	T-bus To Output (IOR)
CLC	Clear Control bit IO state
STC	Set Control bit IO state
CLF	Clear Flag IO state
STF	Set Flag IO state
SFC	Skip if Flag Clear IO state
SFS	Skip if Flag Set IO state
OTx	Output A/B IO state
LIx	Load Into A/B IO state
MIx	Merge Into A/B IO state
EOW	End Of Word IO state
IOS0	IO State 0
PTF	Printer Flag
EBT	HPP: Eight-Bit Transfer \ = Q00000
ITS	HPP: Input to SBUS \ = LIX+MIX
nTTXENB	HPP: T-bus to A/B \ = n(LIX+MIX

Keyboard

KSCANCLK	Scan clock
KSCANDET	Pressed key detected
KCn	Keyboard Columns
KRn	Keyboard Rows
nKSTOP	STOP key pressed
KLS	Keyboard interrupt ack (HP: KB Lights Strobe)
KDBENB	Keyboard Data Bus Enable

Display

DEN	Display Enable
DOFF	Display Off
DCA0..2	Display Column Address
DRELA..G	Display Row Enables Left group
DRERA..G	Display Row Enables Right group
DBANK	Display Bank select
DC[0..7][a..e]	Display Column drives

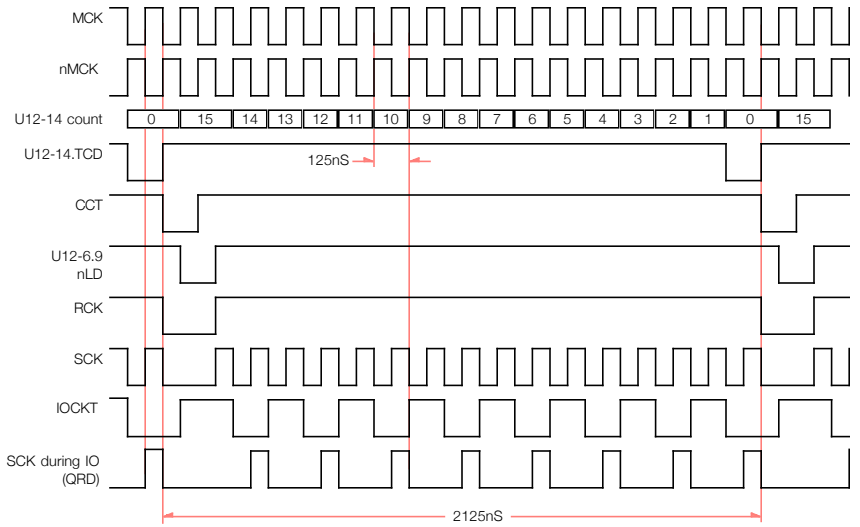
Tape Drive

WCL	Write CLock
WMK	Write MarK
WDT	Write DaTa
WDA	Write Data channel A
WDB	Write Data channel B
RCL	Read CLock
RMK	Read MarK
RDT	Read DaTa
ARA	Analog Read channel A
ARB	Analog Read channel B
CIN	Cassette IN
WPT	Write PermiT
BFD	Blank Feeder Detect
LDR	LeaDeR
CNT	CoNtrol Tape
FTC / FAST	FasT Cassette
RVC / REV	ReVerse Cassette
RNC / RUN	RuN Cassette
STOP	STOP command
LOAD	LOAD register from IO bus
WTC	Write To Cassette
CTM	ConTrol Mode
nPOPC	Power On Pulse Cassette
CTM	Control mode
MFW	Motor Forward
MRV	Motor Reverse
SFW	Solenoid Forward
SRV	Solenoid Reverse
REN	Read Enable
WEN	Write Enable
FLG	FLaG
INT	INTerrupt
DCL	Data CLock

Memory Bank Address Map

Address Decimal	Address Octal	Address Binary	Maps to	Bank	Physical Location
0	00000	000 000 0aa aaa aaa		ROMB00	BASIC ROM
256	00400	000 000 1aa aaa aaa		ROMB00	"
512	01000	000 001 0aa aaa aaa		ROMB01	"
768	01400	000 001 1aa aaa aaa	40000	RAMB0	"
1024	02000	000 010 aaa aaa aaa		ROMB02	"
1536	03000			ROMB03	"
2048	04000			ROMB04	"
2560	05000			ROMB05	"
3072	06000			ROMB06	"
3584	07000			ROMB07	"
4096	10000			ROMB10	"
4608	11000			ROMB11	"
5120	12000			ROMB12	"
5632	13000			ROMB13	"
6144	14000			ROMB14	"
6656	15000			ROMB15	"
7168	16000	001 110 aaa aaa aaa		ROMB16	Card 26a
7680	17000	001 111 aaa aaa aaa		ROMB17	"
8192	20000	010 000 aaa aaa aaa		ROMB20	Cartridge c
8704	21000			ROMB21	"
9216	22000			ROMB22	Cartridge b
9728	23000			ROMB23	"
10240	24000			ROMB24	Card 26b
10752	25000			ROMB25	"
11264	26000			ROMB26	Cartridge a
11776	27000			ROMB27	"
12288	30000			ROMB30	Card 26c
12800	31000			ROMB31	"
13312	32000			ROMB32	Card 26d
13824	33000			ROMB33	"
14336	34000			ROMB34	Cartridge d
14848	35000			ROMB35	"
15360	36000			ROMB36	Cartridge e
15872	37000	011 111 aaa aaa aaa		ROMB37	"
16384	40000	100 000 0aa aaa aaa	01400	ROMB01	ROM Board
16640	40400	100 000 1aa aaa aaa		RAMB0	RAM Board rear
17408	42000	100 01a aaa aaa aaa		RAMB1	"
18432	44000	100 10a aaa aaa aaa		RAMB2	"
19456	46000	100 11a aaa aaa aaa		RAMB3	"
20480	50000	101 00a aaa aaa aaa		RAMB4	RAM Board front
21504	52000	101 01a aaa aaa aaa		RAMB5	"
22528	54000	101 10a aaa aaa aaa		RAMB6	"
23552	56000	101 11a aaa aaa aaa		RAMB7	"
24576	60000	11a aaa aaa aaa aaa		-	unused
32767	77777	111 111 111 111 111		-	max address
		0bb bbb aaa aaa aaa			ROM
		10b bba aaa aaa aaa			RAM
		ppp ppa aaa aaa aaa			page selection

Basic Timing

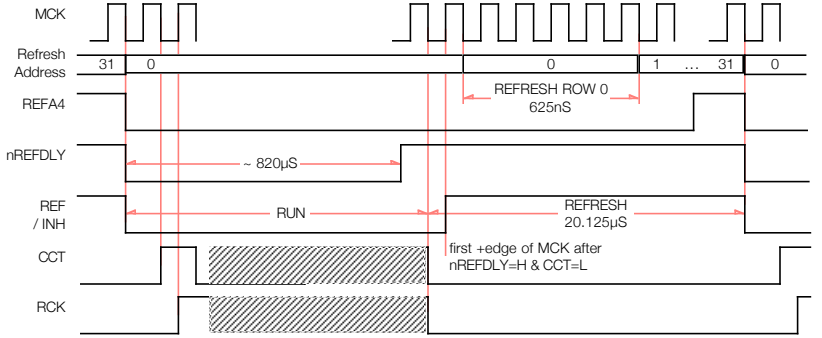


Shown is a full 16-bit microcode cycle, as defined by RCK (ROM clock). The number of pulses of SCK (bit-shift clock) within an RCK cycle, and hence the high period of RCK, is variable from 1 to 16, as determined by the binary code presented by microcode bits CC0,1,2,3.

This is an idealised presentation of the timing relationships, the real-world edge relationships will differ somewhat.

Measured values:
MCK high=60 ns, low=65nS
RCK low=180nS, lagging MCK –edge by 40nS

RAM Refresh Timing



In each refresh cycle, 32 memory access cycles are performed, one for each row in the 1103s. The refresh memory access cycles each require 5 MCK cycles. An additional MCK cycle is needed to transition into the refresh period, thus:
refresh period = (1+ 32*5) * 125nS = 20.125µS.

The run period is determined by the refresh delay monostable, so varies with RC tolerances. The calculated design target for the monostable is 820µS. This will be rounded out to allow completion of an RCK cycle. Each refresh cycle only refreshes half the RAM memory banks however, with a given bank being refreshed on alternate cycles. The effective refresh rate is approximately:
refresh rate = 2 * (820 + 20) = 1680µS, or 595 Hz.

BACKPLANE
TOP VIEW

HP 9830 Computer

Section: Board Layout - Backplane

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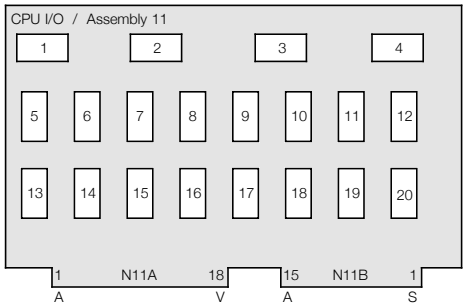

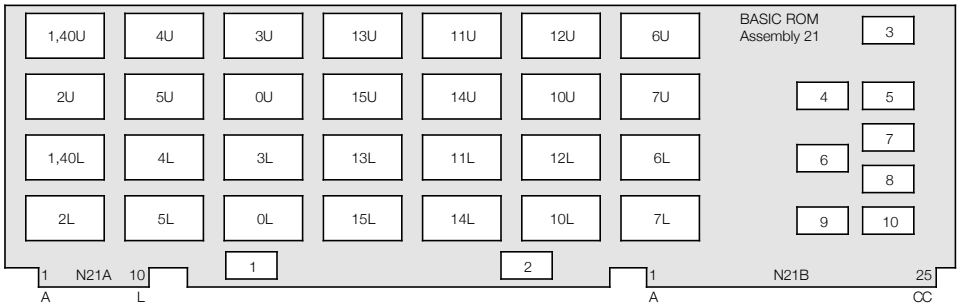

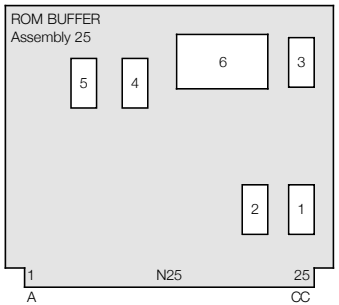

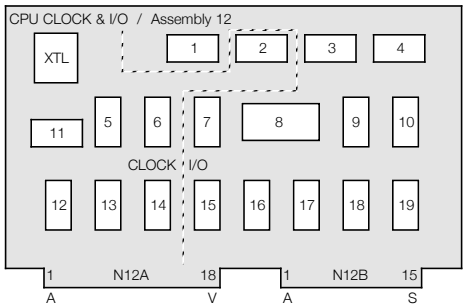

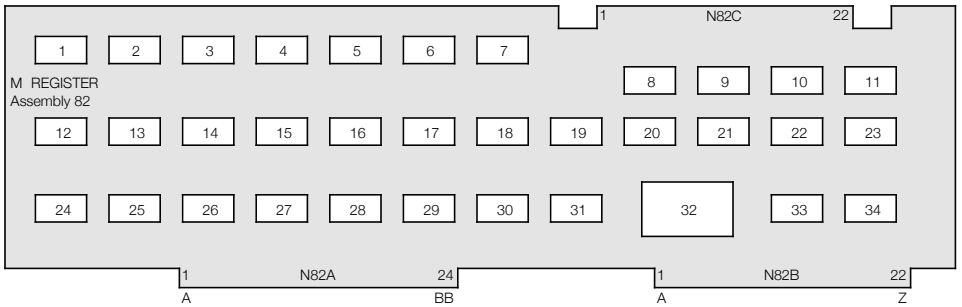

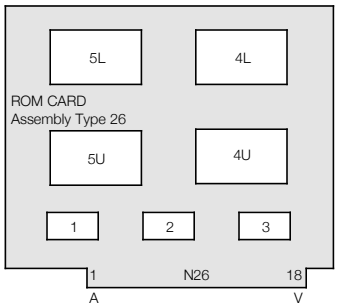

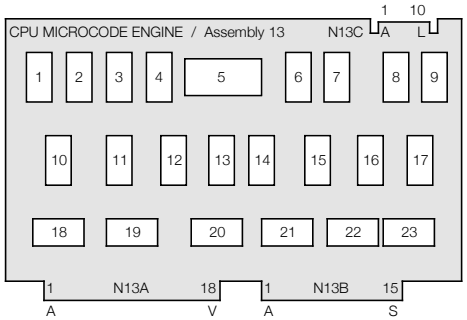

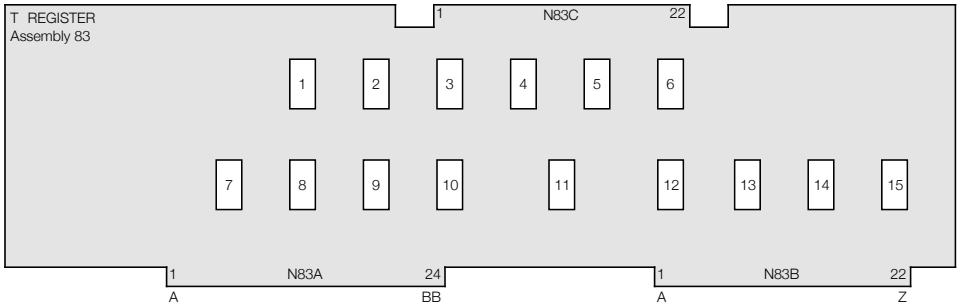

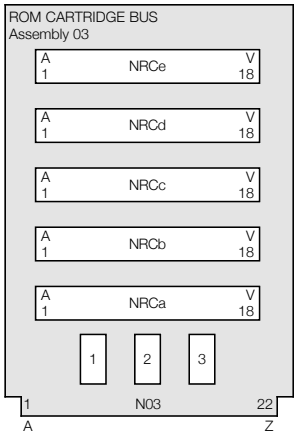

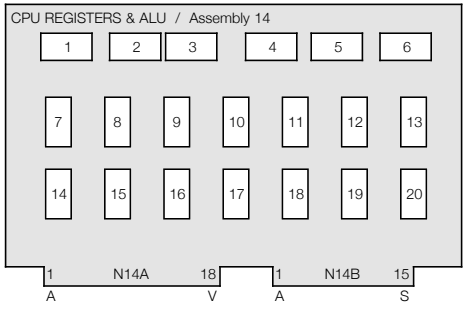

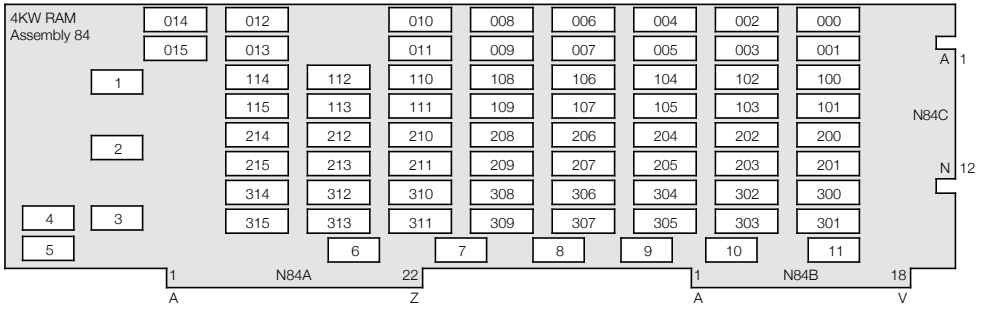

HP 9830 Computer

Section: Board Layout - CPU & Memory

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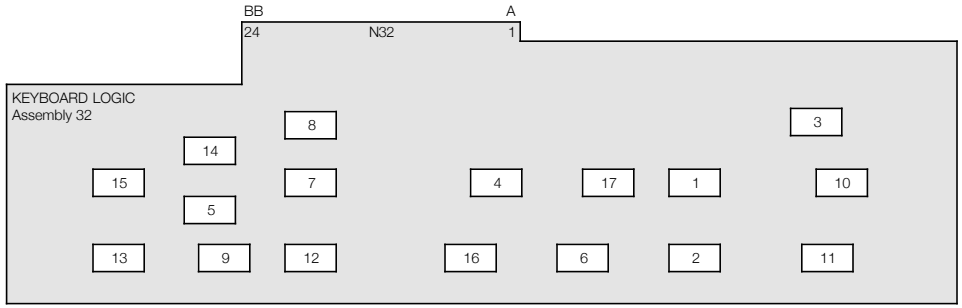
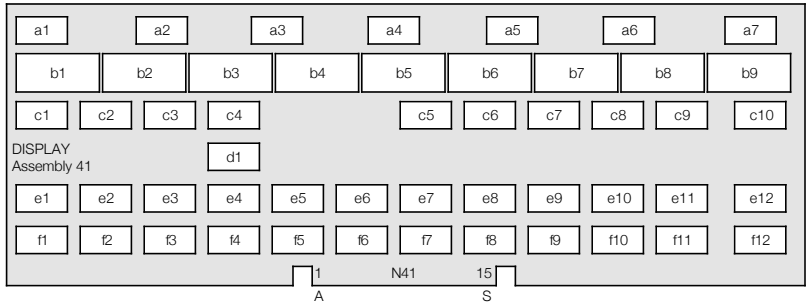
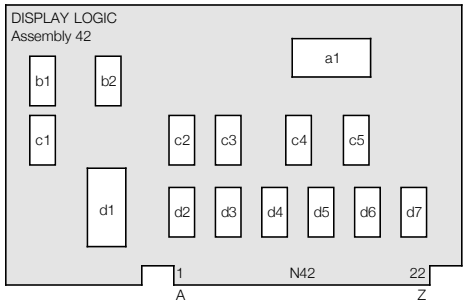
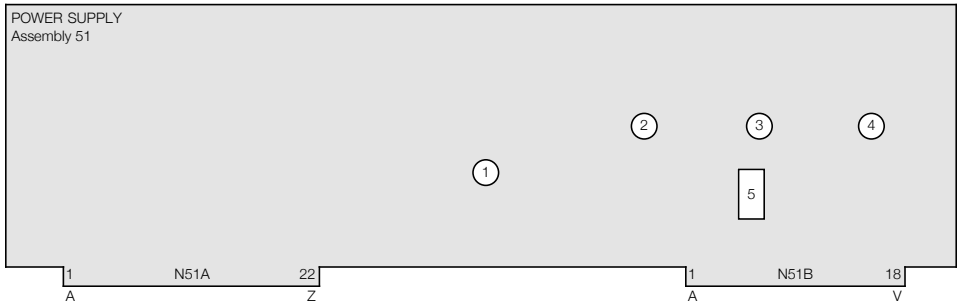
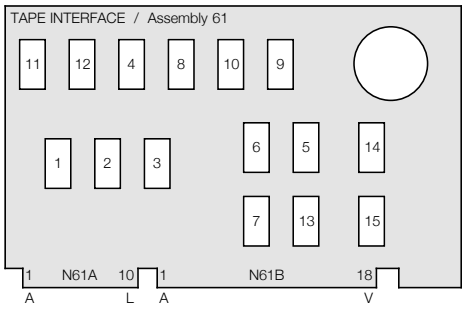
• All boards as viewed from component side.

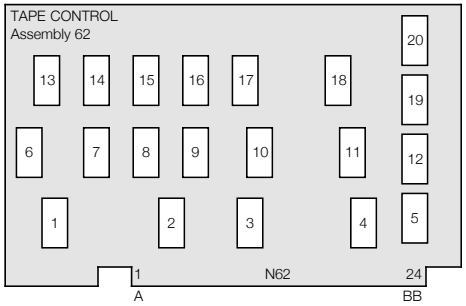

BB
24
N32
A
1
KEYBOARD LOGIC
Assembly 32
8
3
14
15
7
4
17
1
10
5
13
9
12
16
6
2
11

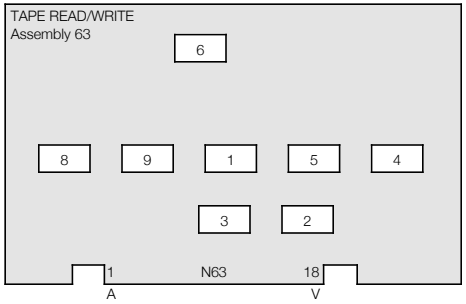

a1
a2
a3
a4
a5
a6
a7
b1
b2
b3
b4
b5
b6
b7
b8
b9
c1
c2
c3
c4
c5
c6
c7
c8
c9
c10
DISPLAY
Assembly 41
d1
e1
e2
e3
e4
e5
e6
e7
e8
e9
e10
e11
e12
f1
f2
f3
f4
f5
f6
f7
f8
f9
f10
f11
f12
1
N41
15
A
S

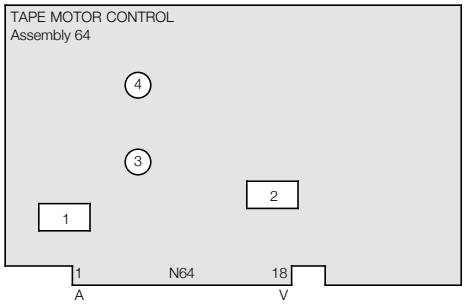

DISPLAY LOGIC
Assembly 42
a1
b1
b2
c1
c2
c3
c4
c5
d1
d2
d3
d4
d5
d6
d7
1
N42
22
A
Z

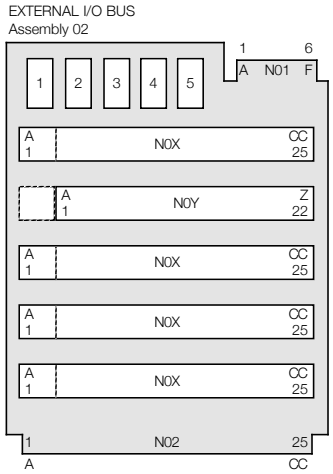

POWER SUPPLY
Assembly 51
1
2
3
4
5
1
N51A
22
A
Z
1
N51B
18
A
V

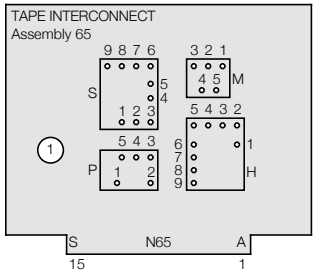

TAPE INTERFACE / Assembly 61
11
12
4
8
10
9
1
2
3
6
5
14
7
13
15
1
N61A
10
A
L
1
N61B
18
A
V

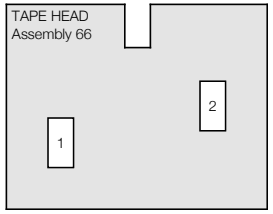

TAPE CONTROL
Assembly 62
20
13
14
15
16
17
18
19
6
7
8
9
10
11
12
1
2
3
4
5
1
N62
24
A
BB


TAPE READ/WRITE
Assembly 63
6
8
9
1
5
4
3
2
1
N63
18
A
V


TAPE MOTOR CONTROL
Assembly 64
4
3
2
1
1
N64
18
A
V


EXTERNAL I/O BUS
Assembly 02
1
6
A
N01
F
1
2
3
4
5
A
1
N0X
CC
25
A
1
N0Y
Z
22
A
1
N0X
CC
25
A
1
N0X
CC
25
A
1
N0X
CC
25
1
N02
25
A
CC


TAPE INTERCONNECT
Assembly 65
9 8 7 6
3 2 1
4 5
M
S
5
4
1 2 3
5 4 3 2
1
5 4 3
6
7
8
9
P
1 2
H
S
15
N65
A
1


TAPE HEAD
Assembly 66
2
1

CPU ALU & REGISTERS N14A

GND	1	A	<
V+5	2	B	<
nTQR	3	C	nTTX
nTTP	4	D	AB
(T0) -	5	E	T0
n(LIx+MIx)	6	F	nTRE
nTTXT	7	H	nPTR
nUTR	8	J	nTBE
SCK	9	K	nAB
nTTXENB	10	L	nXTR
-	11	M	nQTR
-	12	N	-
RCK	13	P	- (RCK)
TBUS	14	R	- (TBUS)
(MCK) -	15	S	nBCD
(nCCT) -	16	T	**MCDIS**
-	17	U	**P0**
-	18	V	-

N14B

T1	1	A	AC0
-	2	B	AC2
-	3	C	Q0
-	4	D	-
T2	5	E	-
-	6	F	MCDIS
SBUS	7	H	- (<)
DC	8	J	AC1
-	9	K	-
-	10	L	T3
QAB	11	M	**BC**
(nPOP) -	12	N	SCB
-	13	P	-
GND	14	R	<
GND	15	S	<

CPU MICROSEQ. N13A

GND	1	A	<
V+5	2	B	<
nTTX	3	C	nTQR
AB	4	D	**nTTP**
nUTR	5	E	**nPTR**
nTRE	6	F	- (MCK)
nWTM	7	H	**nRDM**
nTBE	8	J	- (nINH)
nAB	9	K	SCK
(-) BRC	10	L	**nXTR**
nQTR	11	M	**- (nIPS)**
(XTC) -	12	N	MCDIS
RCK	13	P	**Q9**
Q10	14	R	TBUS
nBCD	15	S	**nCCO**
Q8	16	T	P0
Q4	17	U	**Q5**
Q6	18	V	**Q7**

N13B

AC0	1	A	**Q2**
AC2	2	B	**IQN (-)**
(nIHC) -	3	C	**Q0**
Q3	4	D	**Q1**
QRDb	5	E	QNR
CC4	6	F	**CC8**
CC1	7	H	**CC2**
AC1	8	J	DC
nTTT	9	K	**nTTM**
SC1	10	L	**SC0**
BC	11	M	**QAB**
RCK	12	N	<
nPOP	13	P	nPOP
GND	14	R	<
GND	15	S	<

CPU TEST N13C

PA0	1	A	U13-5.10
PA3	2	B	PA2
PM1	3	C	PA1
SM1	4	D	PM0
SA1	5	E	SA2
-	6	F	SM2
-	7	H	PM2
-	8	J	PM3
SA0	9	K	SA3
SM0	10	L	SM3

CPU CLOCK & I/O N12A

GND	1	A	<
V+5	2	B	<
TTO	3	C	**nSRA**
STF	4	D	nINH
n(LIx+MIx)	5	E	- (<)
-	6	F	MCK
nPTR	7	H	- (<)
nCCT	8	J	XTC
(SCK) -	9	K	**SCK**
nXTR	10	L	- (<)
nCEM	11	M	nIPS
RCK	12	N	<
(>) -	13	P	Q9
-	14	R	-
nCCO	15	S	Q10
(>) -	16	T	Q8
(>) -	17	U	Q5
Q6	18	V	Q7

N12B

(nPTF) -	1	A	<
(Q4) -	2	B	<
nIHC	3	C	<
(>) -	4	D	**QRDb**
CC8	5	E	<
CC4	6	F	<
CC1	7	H	CC2
(-) nCLC	8	J	**IOC3**
LIx+MIx	9	K	**EOW**
Q00000	10	L	QFG
SCB	11	M	**DRC**
RCK	12	N	<
CLF	13	P	nPOP
GND	14	R	<
GND	15	S	<

BACKPLANE NT

TBUS	1	A	nTTXENB
-	2	B	nCEM
nPOP	3	C	nTTXT
V+5	4	D	<
GND	5	E	<
MCDIS	6	F	Q4

CPU I/O N11A

GND	1	A	<
V+5	2	B	<
nSRA	3	C	STF
TTO	4	D	**nSIH**
TBUS	5	E	**nCEOb**
nKSTOP	6	F	nSSI
nCFI	7	H	**DO15**
(-) a1.8	8	J	**DO14**
-	9	K	**DO13**
(nPTF) -	10	L	**DO12**
nDI11	11	M	**DO11**
nDI10	12	N	**DO10**
nDI9	13	P	**DO9**
nDI8	14	R	**DO8**
nDI7	15	S	**DO7**
nDI6	16	T	**DO6**
nDI5	17	U	**DO5**
nDI4	18	V	**DO4**

N11B

nDI3	1	A	**DO3**
nDI2	2	B	**DO2**
nDI1	3	C	**DO1**
nDI0	4	D	**DO0**
Q4	5	E	Q2
Q0	6	F	nPTF
Q1	7	H	Q3
IOC3	8	J	**KLS**
EOW	9	K	BEEP
QFG	10	L	**Q00000**
DRC	11	M	**QNR**
nDO0	12	N	**a4.6 (-)**
CLF	13	P	**nDEN**
nPOP	14	R	a4.9 (-)
GND	15	S	<

ROM BUFFER N25

GND	1	A	<
V+5	2	B	<
V+12	3	C	**ROMB20**
ROMB21	4	D	**ROMB22**
ROMB23	5	E	**ROMB24**
nM13	6	F	**ROMB30**
M9	7	H	**ROMB25**
M10	8	J	**ROMB26**
M11	9	K	**ROMB27**
M12	10	L	**ROMB31**
nAROM	11	M	**ROMB32**
(V+16) -	12	N	**ROMB33**
ROMnA8	13	P	**nROMnA8b**
ROMA8	14	R	**nROMA8b**
nROMA7	15	S	**nROMA7b**
nROMA6	16	T	**nROMA6b**
nROMA5	17	U	**nROMA5b**
nROMA4	18	V	**nROMA4b**
nROMA3	19	W	**nROMA3b**
nROMA2	20	X	**nROMA2b**
nROMA1	21	Y	**nROMA1b**
nROMA0	22	Z	**nROMA0b**
ROMB37	23	AA	**ROMB35**
ROMB36	24	BB	**ROMB34**
GND	25	CC	<

ROM CARTRIDGE BUS N03

nROMnA8b	1	A	nROMA0b
nMR7	2	B	nROMA7b
nMR5	3	C	nMAC
nMR3	4	D	nROMA2b
nMR10	5	E	nROMA4b
nMR8	6	F	-
nMR1	7	H	-
nMR12	8	J	-
nMR6	9	K	nROMA6b
nMR14	10	L	V-12
nMR4	11	M	V+5
nMR2	12	N	GND
nMR0	13	P	GND
nMR9	14	R	nROMA5b
nMR11	15	S	nROMA3b
nMR13	16	T	nROMA1b
nMR15	17	U	ROMB27
nROMA8b	18	V	ROMB22
ROMB35	19	W	ROMB23
ROMB37	20	X	ROMB20
ROMB34	21	Y	ROMB21
ROMB36	22	Z	ROMB26

ROM CARDS N26

V+5	1	A	<
V-12	2	B	**nMR15**
nMAC	3	C	**nMR14**
ROMB<lo>	4	D	**nMR13**
ROMB<hi>	5	E	**nMR12**
-	6	F	**nMR11**
-	7	H	**nMR10**
nROMnA8b	8	J	**nMR9**
nROMA8b	9	K	**nMR8**
nROMA7b	10	L	**nMR7**
nROMA6b	11	M	**nMR6**
nROMA5b	12	N	**nMR5**
nROMA4b	13	P	**nMR4**
nROMA3b	14	R	**nMR3**
nROMA2b	15	S	**nMR2**
nROMA1b	16	T	**nMR1**
nROMA0b	17	U	**nMR0**
GND	18	V	<

ROM CARTRIDGES NRC

nROMA0b	1	A	nROMnA8b
nMAC	2	B	nROMA7b
nMRC7	3	C	nROMA2b
nMRC3	4	D	**nMRC5**
nMRC1	5	E	nROMA4b
nMRC10	6	F	**nMRC8**
-	7	H	nROMA6b
nMRC6	8	J	**nMRC12**
V-12	9	K	**nMRC14**
nMRC2	10	L	**nMRC4**
nMRC9	11	M	**nMRC0**
GND	12	N	<
nROMA5b	13	P	nROMA3b
V+5	14	R	<
nMRC11	15	S	nROMA1b
nROMA8b	16	T	**nMRC13**
ROMB<hi>	17	U	**nMRC15**
ROMB<lo>	18	V	-

- : dash indicates no connection
() : parentheses indicate backplane connection when different from board connection

HP 9830 Computer
Section: Connectors - ROM & CPU
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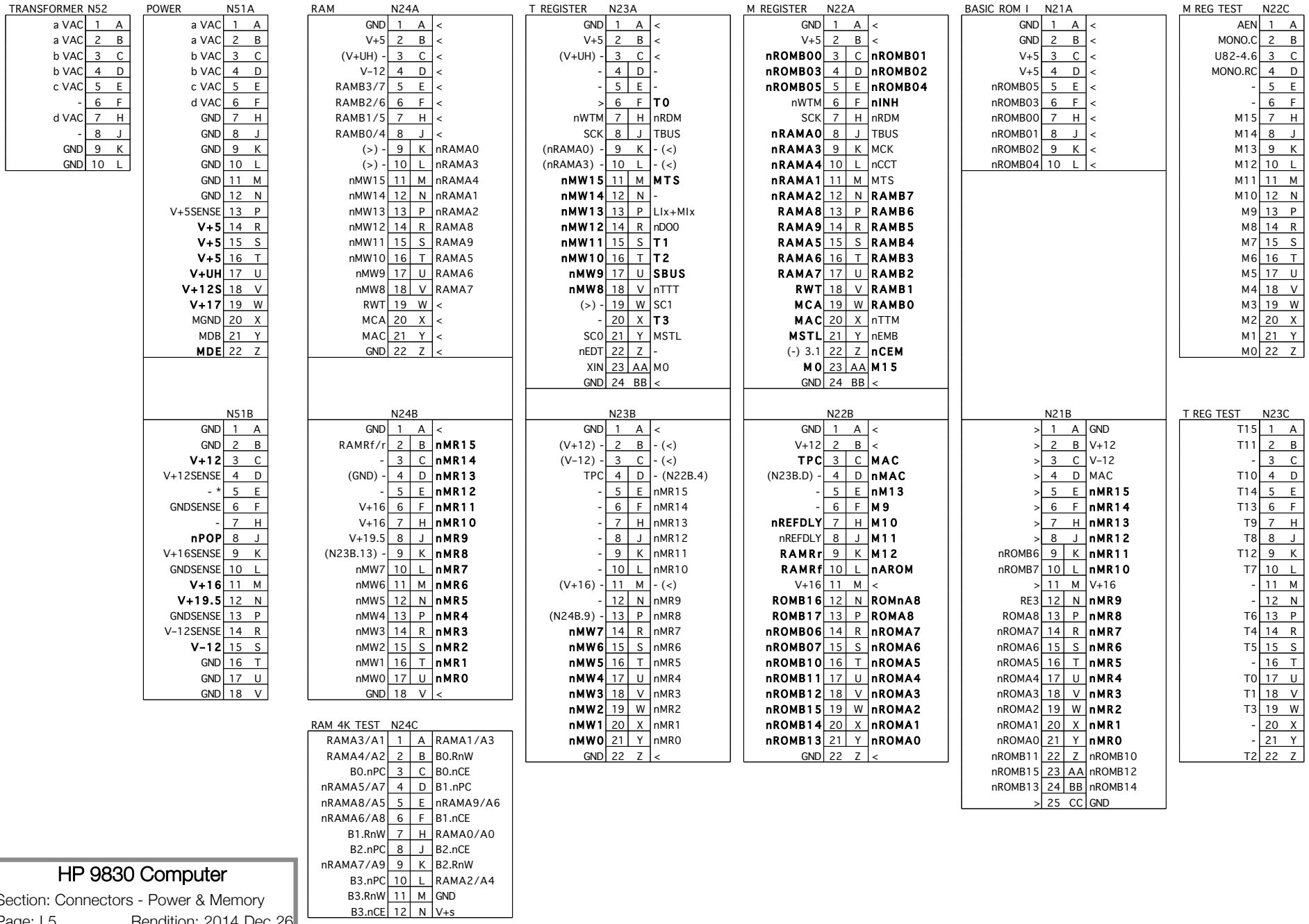

TRANSFORMER N52

a VAC	1	A
a VAC	2	B
b VAC	3	C
b VAC	4	D
c VAC	5	E
-	6	F
d VAC	7	H
-	8	J
GND	9	K
GND	10	L

POWER N51A

a VAC	1	A
a VAC	2	B
b VAC	3	C
b VAC	4	D
c VAC	5	E
d VAC	6	F
GND	7	H
GND	8	J
GND	9	K
GND	10	L
GND	11	M
GND	12	N
V+5SENSE	13	P
V+5	14	R
V+5	15	S
V+5	16	T
V+UH	17	U
V+12S	18	V
V+17	19	W
MGND	20	X
MDB	21	Y
MDE	22	Z

N51B

GND	1	A
GND	2	B
V+12	3	C
V+12SENSE	4	D
- *	5	E
GNDSENSE	6	F
-	7	H
nPOP	8	J
V+16SENSE	9	K
GNDSENSE	10	L
V+16	11	M
V+19.5	12	N
GNDSENSE	13	P
V-12SENSE	14	R
V-12	15	S
GND	16	T
GND	17	U
GND	18	V

RAM N24A

GND	1	A	<
V+5	2	B	<
(V+UH) -	3	C	<
V-12	4	D	<
RAMB3/7	5	E	<
RAMB2/6	6	F	<
RAMB1/5	7	H	<
RAMB0/4	8	J	<
(>) -	9	K	nRAMA0
(>) -	10	L	nRAMA3
nMW15	11	M	nRAMA4
nMW14	12	N	nRAMA1
nMW13	13	P	nRAMA2
nMW12	14	R	RAMA8
nMW11	15	S	RAMA9
nMW10	16	T	RAMA5
nMW9	17	U	RAMA6
nMW8	18	V	RAMA7
RWT	19	W	<
MCA	20	X	<
MAC	21	Y	<
GND	22	Z	<

N24B

GND	1	A	<
RAMRf/r	2	B	**nMR15**
-	3	C	**nMR14**
(GND) -	4	D	**nMR13**
-	5	E	**nMR12**
V+16	6	F	**nMR11**
V+16	7	H	**nMR10**
V+19.5	8	J	**nMR9**
(N23B.13) -	9	K	**nMR8**
nMW7	10	L	**nMR7**
nMW6	11	M	**nMR6**
nMW5	12	N	**nMR5**
nMW4	13	P	**nMR4**
nMW3	14	R	**nMR3**
nMW2	15	S	**nMR2**
nMW1	16	T	**nMR1**
nMW0	17	U	**nMR0**
GND	18	V	<

RAM 4K TEST N24C

RAMA3/A1	1	A	RAMA1/A3
RAMA4/A2	2	B	B0.RnW
B0.nPC	3	C	B0.nCE
nRAMA5/A7	4	D	B1.nPC
nRAMA8/A5	5	E	nRAMA9/A6
nRAMA6/A8	6	F	B1.nCE
B1.RnW	7	H	RAMA0/A0
B2.nPC	8	J	B2.nCE
nRAMA7/A9	9	K	B2.RnW
B3.nPC	10	L	RAMA2/A4
B3.RnW	11	M	GND
B3.nCE	12	N	V+s

T REGISTER N23A

GND	1	A	<
V+5	2	B	<
(V+UH) -	3	C	<
-	4	D	-
-	5	E	-
>	6	F	**T0**
nWTM	7	H	nRDM
SCK	8	J	TBUS
(nRAMA0) -	9	K	- (<)
(nRAMA3) -	10	L	- (<)
nMW15	11	M	**MTS**
nMW14	12	N	-
nMW13	13	P	LIx+MIx
nMW12	14	R	nDO0
nMW11	15	S	**T1**
nMW10	16	T	**T2**
nMW9	17	U	**SBUS**
nMW8	18	V	nTTT
(>) -	19	W	SC1
-	20	X	**T3**
SC0	21	Y	MSTL
nEDT	22	Z	-
XIN	23	AA	M0
GND	24	BB	<

N23B

GND	1	A	<
(V+12) -	2	B	- (<)
(V-12) -	3	C	- (<)
TPC	4	D	- (N22B.4)
-	5	E	nMR15
-	6	F	nMR14
-	7	H	nMR13
-	8	J	nMR12
-	9	K	nMR11
-	10	L	nMR10
(V+16) -	11	M	- (<)
-	12	N	nMR9
(N24B.9) -	13	P	nMR8
nMW7	14	R	nMR7
nMW6	15	S	nMR6
nMW5	16	T	nMR5
nMW4	17	U	nMR4
nMW3	18	V	nMR3
nMW2	19	W	nMR2
nMW1	20	X	nMR1
nMW0	21	Y	nMR0
GND	22	Z	<

M REGISTER N22A

GND	1	A	<
V+5	2	B	<
nROMB00	3	C	**nROMB01**
nROMB03	4	D	**nROMB02**
nROMB05	5	E	**nROMB04**
nWTM	6	F	**nINH**
SCK	7	H	nRDM
nRAMA0	8	J	TBUS
nRAMA3	9	K	MCK
nRAMA4	10	L	nCCT
nRAMA1	11	M	MTS
nRAMA2	12	N	**RAMB7**
RAMA8	13	P	**RAMB6**
RAMA9	14	R	**RAMB5**
RAMA5	15	S	**RAMB4**
RAMA6	16	T	**RAMB3**
RAMA7	17	U	**RAMB2**
RWT	18	V	**RAMB1**
MCA	19	W	**RAMB0**
MAC	20	X	nTTM
MSTL	21	Y	nEMB
(-) 3.1	22	Z	**nCEM**
M0	23	AA	**M15**
GND	24	BB	<

N22B

GND	1	A	<
V+12	2	B	<
TPC	3	C	**MAC**
(N23B.D) -	4	D	**nMAC**
-	5	E	**nM13**
-	6	F	**M9**
nREFDLY	7	H	**M10**
nREFDLY	8	J	**M11**
RAMRr	9	K	**M12**
RAMRf	10	L	**nAROM**
V+16	11	M	<
ROMB16	12	N	**ROMnA8**
ROMB17	13	P	**ROMA8**
nROMB06	14	R	**nROMA7**
nROMB07	15	S	**nROMA6**
nROMB10	16	T	**nROMA5**
nROMB11	17	U	**nROMA4**
nROMB12	18	V	**nROMA3**
nROMB15	19	W	**nROMA2**
nROMB14	20	X	**nROMA1**
nROMB13	21	Y	**nROMA0**
GND	22	Z	<

BASIC ROM I N21A

GND	1	A	<
GND	2	B	<
V+5	3	C	<
V+5	4	D	<
nROMB05	5	E	<
nROMB03	6	F	<
nROMB00	7	H	<
nROMB01	8	J	<
nROMB02	9	K	<
nROMB04	10	L	<

N21B

>	1	A	GND
>	2	B	V+12
>	3	C	V-12
>	4	D	MAC
>	5	E	**nMR15**
>	6	F	**nMR14**
>	7	H	**nMR13**
>	8	J	**nMR12**
nROMB6	9	K	**nMR11**
nROMB7	10	L	**nMR10**
>	11	M	V+16
RE3	12	N	**nMR9**
ROMA8	13	P	**nMR8**
nROMA7	14	R	**nMR7**
nROMA6	15	S	**nMR6**
nROMA5	16	T	**nMR5**
nROMA4	17	U	**nMR4**
nROMA3	18	V	**nMR3**
nROMA2	19	W	**nMR2**
nROMA1	20	X	**nMR1**
nROMA0	21	Y	**nMR0**
nROMB11	22	Z	nROMB10
nROMB15	23	AA	nROMB12
nROMB13	24	BB	nROMB14
>	25	CC	GND

M REG TEST N22C

AEN	1	A
MONO.C	2	B
U82-4.6	3	C
MONO.RC	4	D
-	5	E
-	6	F
M15	7	H
M14	8	J
M13	9	K
M12	10	L
M11	11	M
M10	12	N
M9	13	P
M8	14	R
M7	15	S
M6	16	T
M5	17	U
M4	18	V
M3	19	W
M2	20	X
M1	21	Y
M0	22	Z

T REG TEST N23C

T15	1	A
T11	2	B
-	3	C
T10	4	D
T14	5	E
T13	6	F
T9	7	H
T8	8	J
T12	9	K
T7	10	L
-	11	M
-	12	N
T6	13	P
T4	14	R
T5	15	S
-	16	T
T0	17	U
T1	18	V
T3	19	W
-	20	X
-	21	Y
T2	22	Z

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Section: Connectors - Power & Memory

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TAPE INTERFACE N61A

GND	1	A	<
V+5	2	B	<
nDI11	3	C	**nDI10**
nDI9	4	D	**nDI8**
nDI7	5	E	**nDI6**
nDI5	6	F	**nDI4**
nDI3	7	H	**nDI2**
nDI1	8	J	**nDI0**
(DO12) -	9	K	- (DO13)
(DO14) -	10	L	- (DO15)

N61B

GND	1	A	nBFD
CIN	2	B	**LDR**
nCTMb	3	C	nWPT
nnLDR	4	D	nCIN
ID0	5	E	ID1
ID2	6	F	ID3
ID4	7	H	ID5
ID6	8	J	ID7
CNT	9	K	FLG
nSSI	10	L	nSIH
nCEOb	11	M	**nCFI**
(nKSTOP) -	12	N	nPOPC
nRNC	13	P	BEEP
-	14	R	-
DO12	15	S	DO13
DO14	16	T	DO15
-	17	U	**nINT**
(nDEN) -	18	V	-

TAPE CONTROL N62

GND	1	A	<
V+5	2	B	<
CIN	3	C	WPT
nINT	4	D	LDR
nCTMb	5	E	**nWPT**
nnLDR	6	F	**nCIN**
ID0	7	H	**ID1**
ID2	8	J	**ID3**
ID4	9	K	**ID5**
ID6	10	L	**ID7**
CNT	11	M	**FLG**
nRNC	12	N	nKRWD
nFTC	13	P	**nRVC**
nWTC	14	R	**nPOPC**
RMK	15	S	RDT
nRCL	16	T	**WMK**
WDT	17	U	**WCL**
DO0	18	V	DO1
DO2	19	W	DO3
DO4	20	X	DO5
DO6	21	Y	DO7
DO8	22	Z	DO9
DO10	23	AA	DO11
GND	24	BB	<

KEYBOARD LOGIC N32

GND	1	A	<
KC15	2	B	KR7
KC14	3	C	KR6
KC13	4	D	KR5
KC12	5	E	KR4
KC11	6	F	KR3
KC10	7	H	KR2
KC9	8	J	KR1
KC8	9	K	KR0
KC7	10	L	KSHF
KC6	11	M	nSIH
KC5	12	N	**nDI6**
KC4	13	P	**nDI7**
KC3	14	R	**nDI5**
KC2	15	S	**nDI4**
KC1	16	T	**nDI0**
KC0	17	U	**nDI1**
-	18	V	**nDI3**
KLS	19	W	**nDI2**
DO15	20	X	**nSSI**
DO14	21	Y	**nKSTOP**
DO13	22	Z	DO12
V+5	23	AA	<
GND	24	BB	<

TAPE READ/WRITE N63

GND	1	A	<
V+5	2	B	<
WDA	3	C	**WEN**
WDB	4	D	ARA
WPT	5	E	ARB
AGND	6	F	<
-	7	H	-
(-) DRA	8	J	-
(-) DRB	9	K	-
-	10	L	-
-	11	M	-
nFTC	12	N	-
WTC	13	P	nPOPC
RMK	14	R	**RDT**
nRCL	15	S	WMK
WDT	16	T	WCL
V+12	17	U	V-12
GND	18	V	<

TAPE MOTOR CTL N64

GND	1	A	<
V+5	2	B	<
MRV	3	C	<
MFW	4	D	<
MCM	5	E	<
SFW	6	F	<
SRV	7	H	<
V+17	8	J	<
MGND	9	K	<
MDB	10	L	<
MDE	11	M	<
AGND	12	N	<
LDR	13	P	-
-	14	R	-
nRNC	15	S	-
nFTC	16	T	nRVC
V+12	17	U	V-12
GND	18	V	<

TAPE INTERCONNECT N65

V+12S	1	A	<
SRV	2	B	<
SFW	3	C	<
MCM	4	D	<
MRV	5	E	<
MFW	6	F	<
(-) CHASSIS	7	H	<
GND	8	J	<
V+5	9	K	<
AGND	10	L	<
ARA	11	M	**ARB**
WDA	12	N	WEN
nBFD	13	P	WDB
CIN	14	R	**WPT**
V+12	15	S	V-12

EXTERNAL I/O N02 N0Y N0X

nRDM		1	A		nTTM
MTS		2	B		nEMB
M15		3	C		XIN
GND	1	4	D	A	<
V+5	2	5	E	B	<
T0	3	6	F	C	nEDT
MCK	4	7	H	D	-
nWTM	5	8	J	E	SCK
nDI0	6	9	K	F	DO0
DO1	7	10	L	H	DO2
nDI3	8	11	M	J	DO3
nDI2	9	12	N	K	**nDI1**
DO4	10	13	P	L	**nDI4**
DO5	11	14	R	M	**nDI5**
DO6	12	15	S	N	**nDI6**
DO7	13	16	T	P	**nDI7**
DO8	14	17	U	R	**nDI8**
DO9	15	18	V	S	**nDI9**
DO10	16	19	W	T	**nDI10**
DO11	17	20	X	U	**nDI11**
DO12	18	21	Y	V	DO13
DO14	19	22	Z	W	DO15
nSSI	20	23	AA	X	nSIH
nCEOb	21	24	BB	Y	**nCFI**
GND	22	25	CC	Z	nKSTOP

Note

The external I/O connectors are used with two sets of labels. The full edge connector socket has 50-pins, however most plug-in I/O modules are 44-pin and do not connect to the first 6 pins of the socket.

KEYBOARD MATRIX N31

V+5	1	A	KC0
-	2	B	KC1
KREW	3	C	KC2
(GND)	4	D	KC3
KR0	5	E	KC4
KR1	6	F	KC5
KR2	7	H	KC6
KR3	8	J	KC7
KR4	9	K	KC8
KR5	10	L	KC9
KR6	11	M	KC10
KR7	12	N	KC11
KC15	13	P	KC12
KSHF	14	R	KC13
GND	15	S	KC14

KEYBOARD INTERFACE N34

GND	1	A	<
(nPTF) -	2	B	KLS
nSIH	3	C	**nKSTOP**
nSSI	4	D	**nDI7**
nDI6	5	E	**nDI5**
nDI4	6	F	**nDI3**
nDI2	7	H	**nDI1**
nDI0	8	J	DO12
DO13	9	K	DO14
DO15	10	L	**KREW**
GND	11	M	<
V+5	12	N	<
-	13	P	-
-	14	R	-
(V+12) -	15	S	- (V-12)

DISPLAY LOGIC N42

GND	1	A	<
V+5	2	B	<
nDEN	3	C	DO0b
DRERG	4	D	**DRERF**
DRERE	5	E	**DRERD**
DRERC	6	F	**DRERB**
DRERA	7	H	**DRELG**
DRELF	8	J	**DRELE**
DRELD	9	K	**DRELC**
DRELB	10	L	**DRELA**
DCA0	11	M	**DCA1**
DCA2	12	N	**DOFF**
-	13	P	-
-	14	R	-
DO4	15	S	DO5
DO6	16	T	DO7
DO8	17	U	DO9
DO10	18	V	DO11
DO12	19	W	DO13
DO14	20	X	DO15
V+12	21	Y	V-12
GND	22	Z	<

DISPLAY N41

GND	1	A	<
V+5	2	B	<
DRERF	3	C	DRERG
DRERD	4	D	DRERE
DRERB	5	E	DRERC
DRELG	6	F	DRERA
DRELE	7	H	DRELF
DRELC	8	J	DRELD
DRELA	9	K	DRELB
DCA1	10	L	DCA2
DOFF	11	M	DCA0
DO1	12	N	DO0
DO3	13	P	DO2
DO0b	14	R	<
GND	15	S	<

PRINTER N01

nPACK	1	A	**nPSTB**
nPD3	2	B	**nPD6**
nPD4	3	C	**nPD1**
nPD5	4	D	**nPD2**
GND	5	E	**nPD0**
GND	6	F	-