# OCTANE Technical Report

**Silicon Graphics, Inc.**

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# *Section 1 Introduction*

The OCTANE system delivers a new, dramatically faster, more powerful alternative for those who require state-of-the-art graphics capabilities and massive computing power in a desktop system. A radical new system architecture, focusing on data throughput, has made this significant improvement in performance possible.

The crossbar-based, symmetric multiprocessing architecture employed by the OCTANE system makes the following benefits possible:

- outstanding application performance, especially with the dual R10000 processor option
- true three-dimensional visualization
- real-time manipulation of large images
- real-time simulation involving large data sets
- simultaneous visualization and analysis of large data sets in real time
- interactive modeling and analysis of large, three-dimensional models
- high speed networking
- high, sustainable I/O bandwidth for large amounts of data
- large memory capacity (up to 2GB)
- high, sustainable memory bandwidth

An innovative approach to desktop system architecture was required to solve the system throughput limitations related to standard system architectures. While processor performance has increased over time at an exponential rate, bandwidth has not. This has created a major barrier to efficient performance, by causing lag time in both the processor and graphics systems as they wait for data to continue. Therefore, in order to improve graphics performance and take full advantage of the processor speed available today, Silicon Graphics targeted this problem. OCTANE utilizes a seven port crossbar switch to allow multiple, simultaneous data transfers rather than the one-at-a-time transfers of traditional systems. This delivers very high bandwidth and advanced bandwidth management capabilities. Each port is capable of running at 1.6GB per second peak and 1.2GB per second sustained, while the memory bandwidth is 1GB per second. OCTANE is the first true, desktop implementation of a non-blocking, multiport, crossbar in which every device has its own dedicated port; effectively improving system throughput rates and optimizing processor and graphics efficiency.

Additionally, the dual CPU option allows users to increase their processing efficiency by optimizing compute code. Applications depending on real-time data visualization and cumbersome amounts of data processing benefit especially from this type of system fine-tuning. Multiple applications can run simultaneously, while maintaining interactivity. Many applications can split processes between the processors providing an optimal compute environment for the particular needs of the user.

The enhanced version of the Silicon Graphics high performance graphical subsystem, based on the Indigo$^2$ IMPACT chip set, that is incorporated in OCTANE, provides an exceptionally high

quality of graphics at the desktop. Integrated texture mapping mechanisms and dedicated geometry hardware, combined with industry leading high fill rates and optimized OpenGL, streamline and enhance the graphics capabilities of the OCTANE system. The ability to specify the use of dual CPUs can facilitate maximum graphics performance during the simultaneous computation of non-graphics tasks.

A modular design combined with a number of options make the system highly expandable and suitable for applications with the most demanding desktop configuration requirements. The OCTANE chassis supports dual processor configurations with: four XIO slots for graphics, video, audio, and high speed I/O devices; three optional PCI-64 slots for disk; networking; and more.

The increased total bandwidth of the new system architecture, many times greater than that of Indigo$^2$ IMPACT, combined with the technical excellence of the enhanced IMPACT graphics subsystem and a high degree of expandability offer an unparalleled desktop system for computationally intensive and graphically demanding applications. The system has been designed to support a broad range of manufacturing, entertainment, defense/Simulation and scientific applications, such as:

- industrial design
- modeling
- analysis
- digital prototyping
- 3D animation
- film/video/audio
- broadcasting
- publishing
- geographic information systems (GIS)
- defense imaging
- visual simulation
- oil and gas
- chemistry
- medical imaging

A discussion of the computational needs of each of these industries, the benefits of the OCTANE system, and system configurations and options suited to each, makes up the rest of this section of the report.

## 1.1 Manufacturing

### 1.1.1 Industrial Design

OCTANE high performance graphics workstations provide industrial designers with a highly interactive and creative environment in which to realize their designs. Designers require tools that can help them create stylish, ergonomic, and effective products and communicate their product visions to others. From early ideation sketches through 3D modeling, concept evaluation, prototyping and photo-realistic renderings and animations, the digital medium continues to expand the realm of possibilities available during the industrial design process.

Two-dimensional sketching and 3D paint programs provide industrial designers with the digital equivalents of familiar tools, such as pencils, brushes and air brushes. However, in the digital environment, these tools take on far greater flexibility than is possible in the physical world. Many of these tools use texture mapping to improve visual realism.

Advanced texture mapping techniques are hardware-supported in the OCTANE system, which also has an optional 4MB of dedicated texture memory. The texture memory is a standard feature of the OCTANE/MXI configuration. The OCTANE/MXI fill rate is a desktop industry-leading 133 mega pixels per second; which is significant for tasks requiring the “painting” of large areas, such as 3D digital air brushing. Additional design functionality is made possible thanks to hardware-supported blending operations that simply draw or texture map into the frame buffer with the appropriate transparency.

The power of multiprocessing and hardware texturing made available by the OCTANE system is exploited by programs like Alias|Wavefront StudioPaint 3D™ to provide features such as interactive image processing and real-time brushes. The flexibility of these tools serve not only to increase a designer’s productivity, but also to spark creativity through experimentation with methods that are not possible in the physical world. The interactivity made possible by the OCTANE system is crucial to the viability of any of these tools in the work place.

Evaluating the surface quality of a detailed 3D model may involve the digital equivalent of physically holding a shiny object up to the light and viewing it from every possible angle. This would include being able to rotate it ever so slightly to detect surface flaws made visible by the way light is reflected off the surface or interference between parts. The OCTANE graphics pipeline, including hardware texturing and high bandwidth throughput, combined with programs like Alias|Wavefront Studio™ delivers digital results that can provide such detailed information. Large, complex 3D models can be interactively viewed and manipulated with physically accurate lighting models and environment maps (reflections). In later stages of the design process, the multiprocessing and graphics capabilities of the OCTANE system can be employed to quickly render animations of photo-realistic images for more advanced evaluation and presentation purposes.

In many design situations, high resolution laser scans are employed to produce digital descriptions of existing physical objects. These data sets often contain over a million 3D data points. Interactive work with such data sets relies on the rapid loading, display, and manipulation of huge amounts of data. The high bandwidth data transfer capability of the OCTANE crossbar architecture is instrumental in delivering a viable environment for an industrial designer to work with such huge point clouds interactively.

Additionally, by using industrial design tools made feasible by the OCTANE system, designers can maintain the integrity of their designs by transferring accurate 3D models downstream in the design process. Multiple alternatives can be reviewed with engineers, manufacturers, and market focus groups in the same time it once took to review only a few possibilities.

OCTANE represents a new paradigm in desktop computing by facilitating early convergence of the design and analysis phases of product development. The incorporation of the advanced architecture of Silicon Graphics Origin™ servers, allows OCTANE to offer clean scalability for the entire range of manufacturing tasks from design through production.

### 1.1.2 CAD/CAM Solid Modeling

Digital modeling plays an important role in the design and prototyping phases of advanced product manufacturing processes. Applied correctly, it can dramatically reduce the cost -- in time and dollars -- required to move a product from design to production. Advanced analysis techniques coupled with the OCTANE/SSI dual processor option allow digital models to be tested and analyzed as they are being created. For instance, modelers can test digital models for problems related to strength, thermal effects, assembly conflicts, and larger scale contextual design issues as they are developing the product.

This ability to test a digital model while it is being created can significantly reduce the number of expensive and time-consuming physical prototyping cycles that must be preformed prior to actual manufacturing. Discovering form, fit, and function mistakes as they are made allows corrections to be made immediately and avoids much of the tedious process of searching for and correcting other errors that may have been directly caused by the original error.

The OCTANE/SSI is optimized for solid modeling tasks. There are three key features of the new system architecture that make OCTANE the most powerful solid modeling desktop machine available:

- the MIPS R10000 CPU
- memory bandwidth
- high speed, uninterrupted I/O
- outstanding graphics performance

Most of the leading solid modeling software packages are extremely CPU and memory-intensive. The crossbar-supported, high-bandwidth, low-latency memory of the OCTANE system, coupled with a CPU optimized for application performance, translates directly into faster model regeneration and interference checking, which facilitates more efficient design and testing operations. This in turn leads to higher quality products and a shorter product development time.

The model load times supported by OCTANE are the fastest available on any desktop system. Uninterrupted I/O is made possible by one-to-one connections between crossbar ports effectively creating a dedicated connection between disk and memory. This means that a user can for example, load a model directly from the Ultra SCSI disk to memory, without the loading operation being interrupted by other processes taking place in the system such as the arrival of data over a network connection.

Silicon Graphics has always been known for its powerful graphics accelerators. The OCTANE system provides additional strength to this reputation in the display of large scale, complex 3D solid models. Often the limiting factor in this task is the transformation of three-dimensional model data into the two dimensional data required for display. The OCTANE system employs a hardware Geometry Engine® (960 MFLOPS RDRAM) to perform the transformation of vast amounts of three-dimensional information found in large digital models into an image that appears on the monitor. This hardware geometry engine acts like a powerful co-processor that relieves the CPU of repetitive geometry calculations. Its design avoids some of the trade-offs that are necessarily a part of a general purpose CPU, making it even more efficient than the CPU for geometry computation. One unique feature of the hardware Geometry Engine ASICS of the OCTANE system is that, unlike CPU-based geometry systems, it can be scaled. Adding a second chip yields twice the performance.

Because the OCTANE graphics subsystem is able to process 3D models so quickly, it is important to be able to provide it with data at an equally high rate. The new system architecture supplies the high bandwidth needed to keep the graphics pipeline full. The result is fluid interaction even with very complex assemblies.

The OCTANE/SSI is the ideal desktop machine for demanding professional modeling applications. It incorporates two Geometry Engines, delivering enough power to allow component designers to manipulate and view entire assemblies, test components, and analyze interactions within assemblies all with the same desktop machine.

### 1.1.3 Analysis

OCTANE provides unprecedented power in a desktop system for engineering analysis applications in which the computational demand for rapid processing of huge data sets -- terabytes in some cases -- is crucial. OCTANE is the first desktop computer that can effectively support both design and analysis simultaneously. With OCTANE, it is no longer necessary to ship large simulation jobs off to a mainframe for computation. Design, analysis, simulation, optimization, and visualization can all take place at the same desktop station.

Engineering analysis software is computationally intensive, requiring strong floating-point performance, symmetric multiprocessing, high-speed memory and I/O systems, and 64-bit processing. Leading engineering analysis solutions have historically taken advantage of these capabilities on Silicon Graphics systems with the powerful scalability of the POWER CHALLENGE™ and Origin supercomputers. With the advent of the OCTANE system, many of these advanced capabilities are now available on the desktop.

The dual processor option, coupled with the high performance graphics and I/O subsystems, make OCTANE extremely flexible and an exceptionally productive tool for manufacturing analysis. With OCTANE:

- both CPUs may be applied to an analysis problem, with the graphics subsystem being used for visual analysis; or
- one CPU can be dedicated to analysis, while the other provides the processing power to work interactively with a design model

Most leading solid modeling applications support a seamless integration with advanced engineering analysis packages, facilitating both paradigms. The new non-blocking, multiport,

crossbar-based system architecture eliminates the lag time inherent to the single-path-for-all-data design of traditional shared bus architectures. This results in exceptionally high bandwidth to and from disk and graphics bandwidth, facilitating simultaneous analysis and interactive modeling for the first time on a desktop system.

OCTANE is the first system to provide high performance compute power capable of facilitating the analysis of huge data sets and the visualization of results all in a compact, widely deployable desktop computer.

### 1.1.4 Digital Prototyping

Digital prototyping is an emerging technology pioneered by some of the leaders in the automotive and aircraft industries to optimize designs and reduce costs. With the growing power of desktop computing systems, this technology is moving into more and more areas of manufacturing. Digital prototyping allows engineers to review assemblies and subassemblies, as well as monitor part movements and digitally check for interferences without having to build an actual physical prototype.

Digital prototyping requires the fastest graphics available for real-time interaction with large models. OCTANE provides the most powerful desktop visualization machine available; this allows engineers to verify full assemblies before the first metal is cut.

In dual processor systems, an application that takes advantage of dual CPUs will naturally perform better. For example, an optimized digital prototyping application might assign one CPU to culling objects (removing objects from the scene that cannot be seen), and the other to sending drawing commands to be rendered by the graphics system. 4D Navigator by CATIA/CADAM® is an example of a digital prototyping application that uses this technique, resulting in a significant improvement in running performance.

Most of the leading solid modeling applications provide seamless integration with advanced engineering analysis packages. The high memory bandwidth of the crossbar-based system architecture, coupled with the floating-point performance and 64-bit processing of a MIPS R10000 CPU, support the high level of compute and graphics power needed to run both the three-dimensional solid modeling and the analysis aspects of digital prototyping applications. Dual processors allow complex analyses to take place in the background while an engineer continues to work interactively on the model, dramatically shortening the critical design/test cycle of the product development phase. One processor may even be used as an Intranet server for the revision control system used by a team working on a single assembly, without adversely affecting an engineer's design work on the same machine.

OCTANE supports in-context design of medium to large sized assemblies and subassemblies, such as those involved in designing products in the automotive industry. Components can be quickly reviewed as part of larger assemblies without having to wait for costly physical prototypes. The OCTANE system user is not burdened by the tediously long processing times associated with conventional systems that tie up the CPU. Virtual reality techniques can also be used to identify and resolve design and manufacturing problems early on.

The OCTANE/SSI configuration with dual processors provides the ideal desktop system for digital prototyping applications. Reduced analysis/design iteration time, real-time interaction with models and assemblies, and graphics speed are optimally supported by the symmetric

multiprocessing capabilities and high system bandwidth of the OCTANE system architecture. This translates directly to lower development expenses, shorter development time frames and higher quality products.

## 1.2 Entertainment

### 1.2.1 3D Animation

Computers have become indispensable tools in a number of entertainment related fields, including:

- special effects and post production applications for both film and video
- nonlinear editing, such as that required for creating commercials and editing video
- broadcasting, which can involve weather graphics and other on-air graphics
- game content production

The OCTANE system's revolutionary new system architecture defines the direction for the next generation of desktop visualization workstations. It enables the R10000 processor, also present in the Indigo$^2$ and O2 systems, to perform as much as 70% more efficiently. The high bandwidth, low-latency system allows users to perform tasks never before achievable on desktop computers. Trends in the entertainment industry reflect a growing demand for capabilities such as uncompressed, nonlinear editing and animation of extremely complex, 3D sequences. The OCTANE architecture offers a vehicle for delivering outstanding capabilities to creative professionals in the entertainment industry.

An OCTANE equipped with the high-powered OCTANE/MXI graphics system, dual R10000 processors, OCTANE Digital Video and Compression, and high-speed networking is an ideal workstation for any 3D animator. This collection of technology is powering the next generation of software applications from a number of leading animation developers. It is well suited to complex animation tasks, such as: full scene animations and modeling, or the animation of intricate, organic characters. Dual processors allow animators to simultaneously work with wireframe models and view photo-realistic final rendered images previewed in real time. This is achieved by using one CPU for interactive animation, while the other CPU is occupied with re-rendering the parts of the final image that are changed by the animator. This streamlines the production process and eliminates the waiting time previously associated with test rendering.

The OCTANE Compression card allows animators to play back a motion test sequence at full resolution on an interlaced composite or S-Video monitor without adding an external RAID or DDR. Motion tests can also be played back at full video resolution on the graphics monitor, previewed at video frame rates, or played back in loop mode for synchronization purposes, all without compromising the system performance. This ability to quickly render a set of test images, using the same desktop machine that is used for production, is an extremely valuable and time-saving asset for any production team.

Compressed or full-resolution uncompressed video can also be texture mapped in real time and inserted into a scene to provide rich detail without requiring extensive modeling or animation. Items such as blinking control panels, video billboards, and background settings can now be included as video segments textured onto polygons - all rendered in real time.

Post production processing typically involves combining live footage, audio data, and computer-generated animation and special effects. OCTANE is the first desktop workstation capable of achieving the necessary processing power to support this kind of data-intensive work. Thanks to high speed interconnects between ports provided by its crossbar-based

architecture, OCTANE is able to move an unprecedented quantity of data around the system at speeds previously unattainable in a desktop system.

Game developers can also profit from the graphics and processing performance made possible by the OCTANE system architecture. New games can now be prototyped and played with fully textured, real-time 3D characters. This allows developers to thoroughly evaluate a game concept prior to having the game code written. Once a new concept has been approved, 3D models can best be created and animated using any of the industry-leading software tools that take full advantage of the OCTANE system's unique and powerful computing and graphics capabilities.

OCTANE can increase an animator's productivity dramatically. The ability to test render sequences in real or near real time also allows animators the creative freedom to test a wider range of options without compromising on other aspects of production. The interactive performance of OCTANE coupled with the ability to preview sequences in a form approaching final rendered quality and frame rate helps eliminate guess work. Additionally, support for simple, on-the-fly compositing between live video and computer-generated animation make OCTANE a natural choice not just for high end entertainment applications, but also for fast turn around industries such as news broadcasting.

### 1.2.2 Film/Video/Audio

Real-time, nonlinear, uncompressed, multistream, online editing is now possible at the desktop level thanks to the radically new OCTANE system architecture. The seven port crossbar-based system replaces the one-after-the-other processing bottleneck of traditional system architectures, with symmetric multiprocessing. In combination with a memory bandwidth designed to keep the R10000 processors running flat out, this makes OCTANE the first desktop system capable of supporting uncompressed, multistream editing.

The function of the crossbar switch is similar to that of a video router. It allows data to flow inside the system without interruption. The crossbar contains bandwidth management hardware that can dedicate system resources to ensure that audio and video streams are processed in real time. The high bandwidth of the crossbar (1.6G per second per port peak and 1.2GB per second per port sustained) can handle many simultaneous streams of uncompressed video.

OCTANE provides two channels of 10-bit CCIR-601 video in and out, as well as disk interfaces (such as Ultra SCSI and Fibre Channel) fast enough to store two streams to disk in real time. The base system comes equipped with two Ultra SCSI buses, and three internal 3.5" drive bays that can store up to 27GB of data. Additional Ultra SCSI or Fibre Channel interfaces can be added through PCI or the high-speed XIO bus. Video processing is supported by the OCTANE graphics subsystem.

The OCTANE Digital Video option provides dual input and dual output channels of SMPTE 259M digital video, CCIR serial digital video. The video can be PAL or NTSC timing and 8- or 10-bits per component. The two 4:2:2 inputs can be used together for dual linked signal with video and key. It also supports genlocking and has a blender/keyer which supports chroma and luma keying and blending of live CGI with video. Additionally, a high quality YUV/RGB colorspace converter and video texture port are standard features of the board. This allows real-time, high quality colorspace conversion and the use of live video as a texture map on any 3D

geometry. This translates to true, high quality, 3D digital video effects, unlike those produced by most black box solutions, which rely on inferior 2D, coefficient-based transformation tricks.

For film applications, OCTANE supports real-time manipulation on 1Kx512 streams and real-time display of 2Kx1K - high density television resolution. The OCTANE Compression option is also available for those applications that deal with films requiring greater resolution. It supports one or two real-time video streams at up to 2:1 JPEG compression.

OCTANE provides hardware-supported synchronization between audio and video streams. The baseline audio capabilities of the OCTANE workstation are a generation ahead of the competition. The powerful audio capabilities of OCTANE include 18-bit analog stereo I/O, 24-bit AES I/O (stereo) and 24-bit ADAT Optical I/O (8 channels). The sample rates are adjustable and can be locked to external time bases or to the internal video timing reference bus.

The OCTANE family of workstations support professional video, film, and audio work to a degree never before possible with a desktop computer. Uncompressed nonlinear editing, film resolution effects and real-time interaction with complex 3D scenes are just some of the many solutions powered by the technical innovations of the OCTANE system.

### 1.2.3 Publishing

The advantages of digital media in terms of speed, functionality and flexibility for publishing, prepress and related disciplines are well known. The new OCTANE system architecture offers industry-leading advances in key areas of system functionality relevant to these applications. Data handling speed, supported by true multiprocessing capabilities; superior, hardware-based image processing; and hardware-supported texture mapping are just some of the important features that OCTANE offers.

Because the size of graphic data can be very large -- 300 to 600 dpi for simple pixel images can quickly add up to gigabytes worth of data -- the ability to transfer data quickly and efficiently around the system becomes crucial to interactive work and rapid display update. The bottleneck commonly associated with this data transfer has been eliminated by the new crossbar-based architecture of the OCTANE system.

The OCTANE crossbar, in which every device has its own dedicated port, is the first truly non-blocking, multiport, crossbar implementation in a desktop system. It supports direct, simultaneous, port-to-port data streams of 1.6GB per second peak and 1.2GB per second sustained. These high speed data paths form disk-to-memory and memory-to-graphics subsystem, allowing processors and the graphics board to run more efficiently.

Fast image processing capabilities are a prerequisite for any system supporting advanced imaging, enhancement, and filtering features, such as: color correction, painting, retouching, drawing, and image compositing. Most image processing operations done on the OCTANE system are hardware-accelerated through the OpenGL API. The optimized interface of OpenGL on Silicon Graphics systems insures maximum possible graphics and imaging performance. The highly effective OCTANE system architecture and OpenGL interface provide unprecedented image processing capabilities in a desktop machine.

Two-dimensional texture mapping supports interactive image manipulations, such as rotation and zooming. It is also the most efficient method of implementing paint brushing with large air brushes, because the fastest method to display pixels on the screen is to texture map them from texture memory on to the frame buffer. The associated fill rate on an OCTANE/MXI is about 133 Mega Pixels per second; improved from approximately 119 Mega Pixels per second on an Indigo$^2$ Maximum Impact. Barco Graphics, DALiM Imaging, Contex, and Heidelberg Prepress depend on the power of hardware texture mapping to satisfy their prepress needs.

Color conversion is specifically supported in two portions of the image processing pipeline of the Impact graphics subsystem. Linear color space conversions can be accomplished by means of a color matrix, while nonlinear color space conversions can be performed via a three- or four-dimensional lookup table and the texture subsystem.

Multiprocessing and expandability are two important features of the OCTANE system. The dual processor option allows one CPU to be assigned the task of reading data off the disk, while the other is occupied with feeding the graphics subsystem. One CPU might also be used to handle batch processes, such as lamination, auto trapping or prepress color separation, while interactive editing independently utilizes the second CPU. Multiple PCI slots make connecting hot swappable RAIDs and third party boards for scanners, image setters, and other external devices very convenient.

OCTANE/MXI and OCTANE/SI with texture, both with the dual processor option, are ideal desktop stations for publishing, prepress, and related disciplines that deal with text, image and graphic data. High speed data transfer capabilities combined with the industry-leading OpenGL programmable Impact Graphics subsystem, advanced multiprocessing capabilities and a high degree of expandability make OCTANE an excellent choice in desktop systems for this industry.

## 1.3 Defense/SImulation

### 1.3.1 Defense Imaging

OCTANE provides a desktop alternative for defense applications that typically require the best possible balance between processor speed and data resolution. The new crossbar-based architecture supports high speed, multiprocessing that dramatically improves the efficiency of the overall system by effectively removing the one-at-a-time, data transfer bottleneck built into conventional desktop systems. This results in the kind of computation and graphic speed necessary to power complex analysis, simulation, and training applications. It is the ideal desktop station for a wide array of tasks, including:

- situational assessment
- mission planning
- intelligence analysis
- previewing
- simulation
- rehearsal
- space operations
- satellite tracking
- animated satellite weather imagery

The OCTANE system allows aerospace and defense customers to create large, detailed models interactively with virtual prototyping and virtual manufacturing applications. Software, such as ENVISION and IGRIP® by Deneb Robotics, provide much greater fidelity in physics-based engineering models by taking advantage of the unique features of the OCTANE system architecture. The kinematic and dynamic properties of the mechanisms support real-time reactions to immersed participant input.

The new, crossbar-based architecture of the OCTANE system facilitates unprecedented data transfer rates for a desktop machine by replacing conventional transfer mechanisms with the first truly non-blocking, symmetric multiprocessing, multiport crossbar in a desktop system. The resulting high system bandwidth (1.6GB per second per port peak and 1.2GB per second per port sustained) provides substantial improvements in performance for a wide array of applications.

Advanced, hardware-supported texture mapping techniques, combined with the industry-leading graphics subsystem and an optimized OpenGL interface, allow the huge amounts of data supplied by satellites and other sources to be combined with three-dimensional models and other information at speeds never before possible with a desktop machine. Dual processors allow one processor to be dedicated to feeding the graphics subsystem, while the other takes care of analysis computations and other tasks. This means a higher guaranteed frame rate for the often oversized data sets involved in defense applications; an asset of particular importance for simulation and training applications.

Many of the OCTANE XIO options can make the system even more attractive for defense industry applications. 4-port Ultra SCSI channels allow a large array of additional disk drives to be added to the system for the massive amounts of data that typically have to be accessed by

defense applications. An alternative to SCSI for external disk arrays is the much faster, fiber optics-based Fibre Channel. Presenter, a flat screen 16-bit, 1280x1024, high resolution screen, makes the OCTANE deployable even at difficult sites - for instance, a remote navy base, or the back of a truck.

The availability of massive computing power, huge system bandwidth, and industry-leading graphics, all in an affordable desktop model, make OCTANE an attractive choice for the wide variety of highly data-intensive tasks that define most defense applications. OCTANE/MXI with integrated texture memory or OCTANE/SI with the 4MB of optional texture memory are the best configurations for meeting defense industry needs.

### 1.3.2 Visual Simulation

The OCTANE system provides the compute power and bandwidth required for data-intensive simulation tasks. Real-time, deterministic simulation is key to any successful simulation application where quality equates to the ability to maintain the best possible picture at a prespecified framework. For an operator-in-the-loop simulation, this means a guaranteed frame update rate of 30Hz or greater, in order to avoid distracting visual anomalies. Training and engineering analysis simulators depend on this to closely simulate real life situations and conditions. Typical visual simulation applications include: flight and driving simulators; aircraft part task training; ship bridge training; and engineering analysis simulators that evaluate such things as pilot work load or performance.

Sophisticated texture mapping techniques combined with a high fill rate reduce dependence on extremely complex geometric models, although it is still important to maintain good geometry performance. OCTANE incorporates the industry-leading desktop geometry and fill rates introduced in the Indigo$^2$ IMPACT, with streamlined texture mapping performance via 4MB of dedicated, high-speed texture memory. This significantly increases the speed at which individual frames can be generated. The new crossbow-based architecture increases system bandwidth, which enables considerably faster memory access for those scenes that require larger texture data bases. This translates into a higher quality image at a set, guaranteed frame rate.

The multiple processor configuration of OCTANE allows one processor to be assigned exclusively to rendering tasks, while the other handles all non-graphic tasks including analysis. Typically operator input is fed to the kinematics (or motion) model for conversion, processed based on a physical model, and the results -- a new position and attitude -- are generated. This is done for both human operator controlled and computer operated vehicles and objects. The dual processor configuration allows these calculations to be done without interfering with the actual rendering process.

Taking advantage of the REACT$^{TM}$ real time extensions can also provide non-degrading processing priorities, improved system latencies and processor/memory locking, all of which add up to a system that is able to deliver superior, consistent, real-time behavior for simulation tasks.

The dual head option typically allows the texture equipped head to process texture, while the other takes care of user interface controls. Both heads support 24-bit color and hardware-accelerated geometry. The multiple channel option can also be used to route results to more than one screen to simulate wrap-around views of a scene.

OCTANE systems will be used in a number of different capacities, such as modeling stations to build scenes required for simulations; image generators for scene simulation in both single and multiple-window views; instructor and operator control stations; and compute stations for physics-based dynamic models.

### 1.3.3 Geographic Information Systems (GIS)

OCTANE is the first desktop system ideally suited to support GIS professionals as they link, analyze, and manipulate massive data sets containing geographically referenced resource data. GIS software must facilitate interaction with numerous types of geographically related data, including topographic, demographic, utility, facility, image and other types of data that are commonly part of a GIS data set. The data must also be displayed at an appropriately fast rate to support interactive work. Typically, more than one of these types of data -- terrain, maps, roads, buildings, symbolic markers, etc. -- must be displayed simultaneously. Dual processor OCTANE/SI with texture and OCTANE/MXI provide optimized hardware support for software that delivers such functionality.

The two most crucial aspects of a GIS system are fast data paths and fast graphics. OCTANE delivers both at a level never before supported in a desktop system. The crossbar-based IO architecture avoids data transfer bottlenecks associated with conventional desktop systems by furnishing remarkably high bandwidth between the various subsystems. This allows data delivery at an unprecedented rate and dependability.

Fast graphics, including advanced hardware-supported texture mapping techniques, allow huge data sets to be interactively manipulated two- and three-dimensionally. On OCTANE, most image processing operations are hardware-accelerated through the OpenGL API. This allows programmers to easily take maximum advantage of graphics and image performance potentials, smoothing three-dimensional data roaming and improving the overall graphics capability of the system.

Multiple layers of both two- and three-dimensional data are sent from disk to memory and from memory to the graphics subsystem; where hardware image processing occurs. Operations that enhance raster data, such as Landsat or aerial images, are extremely data-intensive. Sharpening, edge detection, and complex feature extraction, like finding a corn field based on multispectral data, require the IO bandwidth and graphics power that OCTANE provides.

The dual processor option allows one processor to deal with transferring data from the disk, while the other is dedicated to feeding the graphics subsystem for processing and display. Multiprocessing also improves batch processing of multispectral data that is not displayed. For extremely demanding data delivery, the multiport Ultra SCSI option provides fast access to data at over 80MB per second.

For serious GIS applications involving multiple layers of data that require two- and three-dimensional interactivity and rapid frame updates, the OCTANE system provides an exceptional desktop option. Dual processor OCTANE/SI (with the 4MB texture option) and OCTANE/MXI (with built in dedicated texture memory) both offer the data access and graphics power required for handling the complex and oversized data sets typical of GIS projects.

## 1.4 Sciences

### 1.4.1 Oil and Gas

The OCTANE system is ideal for exploration and production tasks related to the energy industry. It allows extremely data and compute intensive geological applications involving huge geologic databases, reservoir characterization tasks, mapping and modeling to be dealt with on the desktop. Other energy related applications, such as seismic acquisition, seismic processing, and seismic interpretation, as well as reservoir engineering, statistical analysis, refinery and platform design, engineering analysis, and process simulation also benefit from the OCTANE system's generous memory bandwidth and high speed, uninterrupted I/O.

The characteristically large data sets of 1GB and more that are required for most oil and gas related visualization and analysis tasks are handled with revolutionary ease by the OCTANE desktop system. Its new crossbar-based architecture supports multiple data streams, thus avoiding the lag time caused by conventional desktop routing systems. Large data sets can be accommodated by three 3.5" drive bays of internal disk storage, which can provide a combined total of 27GB of disk space. The dual CPU configuration option available with OCTANE, combined with the crossbar system architecture, guarantees substantially higher performance efficiency and speed.

Particularly data- and processor-intensive tasks such as data roaming can be handled at a remarkably faster pace, thanks to more efficient data and bandwidth management made possible by the crossbar. Symmetric Multiprocessing, facilitated by the crossbar, allows data to flow from disk to memory and from memory to graphics without degrading lag time; both processes are able to run at full speed without interfering with each other. Volume roaming, used to magnify interactively selected portions to a data set being visualized, can operate at rates up to 50 times faster than that which is possible on a system based on traditional desktop architecture.

The OCTANE system provides the memory bandwidth required to keep the R10000 processor(s) running flat out, boosting overall application performance and data handling capacity. This combined with its industry-leading graphics system make it an ideal system for data-intensive oil and gas applications, including volume rendering and roaming.

### 1.4.2 Chemistry

OCTANE workstations are powerful and productive interactive desktop systems for chemical and pharmaceutical customers. OCTANE combines outstanding three-dimensional visualization with high-end number crunching capabilities. The enormous compute demands of molecular modeling and process simulation -- together with the extraordinary information management requirements of chemical database mining, structure elucidation, and bioinformatics -- greatly exceed the capacity of conventional desktop computers. The radically new system architecture employed in OCTANE changes that by replacing the one-at-a-time data transfer mechanism of common desktop systems with a multiport crossbar. This effectively allows the processors and graphics subsystem to work flat out; dramatically improving overall system performance.

For customers studying proteins, polymers and other large molecules using molecular modeling, molecular visualization, X-Ray and NMR Structure Determination and using advanced quantum chemistry and other computational chemistry and bioinformatics methods, OCTANE workstations are an ideal balance between computing capabilities and the highest level of three-dimensional graphics. OCTANE workstations offer:

- the availability of over 800 chemistry and biology specific applications, including parallelized applications
- outstanding application performance with dual R10000 processors
- true three-dimensional visualization
- fast networking
- large I/O capability
- high, sustainable I/O bandwidth
- large memory capacity (up to 2GB)
- high, sustainable memory bandwidth
- the availability of the full range of SGI collaborative and desktop tools

The dual processor option facilitates the ability to interactively run graphics from one CPU while running compute jobs on the other. The R10000 processor provides outstanding uni- or multiprocessor performance for molecular dynamics or mechanics applications, homology modeling, or the study of electronic structures using quantum methods.

The OCTANE system's industry-leading graphics subsystem and hardware-supported texture mapping solve a wide range of visualization needs, including Stereo-in-a-Window and high resolution stereo viewing. Like all Silicon Graphics products, OpenGL runs optimally on the OCTANE system, allowing programmers to easily take advantage of a number of unique Impact graphics features and control the performance of the graphics portion of their applications.

OCTANE is also attractive as a client and server system for customers needing to access and serve chemical compound and structural databases such as: ISIS/Host by MDL; Unity by Tripos; RS3 by Oxford Molecular; C2 Catalyst by MSI; ChemX/Diversity by Chemical Design; or Thor and Merlin by Daylight CIS. Thanks to the high system bandwidth provided by the crossbar-based architecture, OCTANE is able to provide:

- fast local processing power for creating, submitting and analyzing queries
- fast local processing power for serving departmental databases
- parallelized two-dimensional, three-dimensional and reaction searching in applications like ISIS/Host and Unity
- outstanding network connectivity
- up to 2GB of memory for in-core searching, such as those performed by Daylight CIS applications
- and outstanding data mining and data visualization functionality

For computational biologists manipulating and analyzing sequences of DNA and performing "structure prediction" using techniques like homology modeling and protein or crystal structure prediction, OCTANE offers a number of advantages. It provides: outstanding local

CPU performance and scalable parallel performance on a wide range of bioinformatics applications like FASTA, BLAST, Smith Waterman and other homology search tools; fast network access to intranet and Internet application servers; biological desktop and integration software; leading genetic database systems for managing high-throughput bioinformatics environments; complete use of the SGI Cosmo web execution and development environments.

OCTANE is the ideal desktop workstation for chemistry research, teaching, and application tasks. The well-balanced high speed computational power and industry-leading three-dimensional graphics facilitated by the new crossbar-based, high bandwidth system architecture are without compare. Symmetric multiprocessing makes typically oversized data sets accessible at rates never before seen in a desktop workstation. OCTANE streamlines the way things are done by making simultaneous analysis and real-time visualization of results possible.

### 1.4.3 Medical Imaging

Many sophisticated data acquisition devices are now available for gathering critical information for clinical diagnostic and medical treatment planning purposes. Image precision and speed are both crucial aspects of medical imaging. Time spent acquiring data from individual patients is very expensive. This, combined with the need for highly accurate images, means that data acquisition has to happen at the highest possible speed and volume. As the resolution of diagnostic images increases and the time available for acquisition shrinks, systems that collect, process, and display the data must be able to provide sufficient and reliably consistent computational power and data processing speed.

OCTANE supports standard industry data acquisition and manipulation procedures exceptionally well. It performs routine procedures efficiently, such as processing data collected by a medical data acquisition device in order to quickly supply alternate two- and three-dimensional views of an entire data set. Arbitrarily oriented slices of acquired medical data sets are generated interactively and viewed from any angle. Another core functionality fully supported by OCTANE is interactive windowing. Subtle changes in data can be differentiated via simple, interactive adjustment to the lookup table.

OCTANE is also the industry-leading desktop system for emerging, sophisticated, 3D visualization techniques. It supports interactive surface and volume rendering, which facilitate interactive visualization of volumetric representations of data sets. Although these techniques will not replace the diagnostic value of cross-sectional images in most cases, they will become invaluable tools in cases involving complex topologies, such as tracking vessels involved in aneurysms; tracking gyral convolutions in neurosurgical cases; and preparing and performing maxillofacial surgical applications. These techniques can greatly enhance the diagnostic process and treatment effectiveness in such cases.

NMR, MRI, CT, US, PET, and SPECT are just a few of the systems that will benefit from the OCTANE system's unique data processing features. The dual CPU option and high bandwidth design provide the necessary power and speed to support high-end medical imaging needs. The OCTANE system can be used during the data acquisition and reconstruction phase as a console for diagnostic scanners. Dedicated CPU, priority I/O and guaranteed bandwidth make it a highly reliable solution for use in the acquisition phase. The OCTANE system's superior graphics capabilities also make it an ideal vehicle for two- and three-dimensional visualization,

interactive viewing, and manipulation of acquired medical data for diagnostic and treatment purposes.

# *Section 2 System Architecture*

## 2.1 Architectural Overview

The design of the OCTANE system sought to address issues such as bus bandwidth, true support for real-time digital video and audio streams, and system modularity. In order to solve the bus bandwidth limitations common in shared-bus architectures, it became necessary to design a system which did not adhere to the shared-bus paradigm. In addition, the new system architecture had to accommodate the large bandwidth required to support these real-time data streams. The idea of system modularity became necessary in order to support future generations of processors, memory, and I/O devices with a minimal amount of re-design. The following sections discuss some of the design principles and techniques used in the OCTANE system.

### 2.1.1 Bus Bandwidth and Frequency

The majority of bus architectures on the market today are known as shared-bus architectures. Some of the more common include PCI, EISA, and AT. In a shared-bus architecture, all of the peripheral devices connect to the bus through one set of wires which are routed across all of the connectors. These wires are in turn shared by all of the peripheral devices.

Bus bandwidth is defined as the number of bits which can be transferred between the peripheral and the system during a given time period, usually noted in Megabytes per second (MB per second). Bus bandwidth is determined by two variables; the number of bits supported, and the frequency at which the bus operates (bits x frequency). There are two common techniques for increasing bus bandwidth in a shared-bus system: increasing frequency, and increasing the number of bits or width of the bus.

All peripheral devices in the system must share this bandwidth. While increasing frequency can offer some initial performance improvement, having multiple distributed loads along a single set of wires limits the maximum frequency at which these wires can be driven. In a shared bus architecture, frequencies above approximately 50MHz become impractical as signal integrity is greatly diminished.

Another common technique is to increase the size of the bus. Common bus sizes are 8-, 16-, 32- and 64-bits. Going to 128-bits is somewhat impractical because the device becomes dominated by the physical bus connections required to facilitate these wide data paths. This in turn requires larger more expensive packages to support these large bus sizes.

#### 2.1.1.1 The Crossbow Solution

The Silicon Graphics OCTANE system uses a mechanism called a crossbar switch, incorporated into the *Crossbow* ASIC, to provide solutions for both the frequency and bandwidth problems.

The OCTANE system addresses the signal integrity problems which arise at higher frequencies by using dedicated connections between the peripherals and the Crossbow ASIC. This solution allows two devices to talk to one another over a pair of 16-bit unidirectional point-to-point links running at an effective 400MHz data rate using both edges of a 200MHz clock. In most computer systems information is transferred only on the rising edge of the clock. In an environment operating at 200MHz, a rising clock edge occurs every 5 nanoseconds (nS). This is called the clock period. The Crossbow ASIC not only transfers data on each rising edge of the clock, but also transfers data on each falling edge of the clock. This means that data is transferred every 2.5 nS, which equates to a 400MHz data transfer rate. Figure 2.1 shows how data is transferred relative to the 200MHz clock.

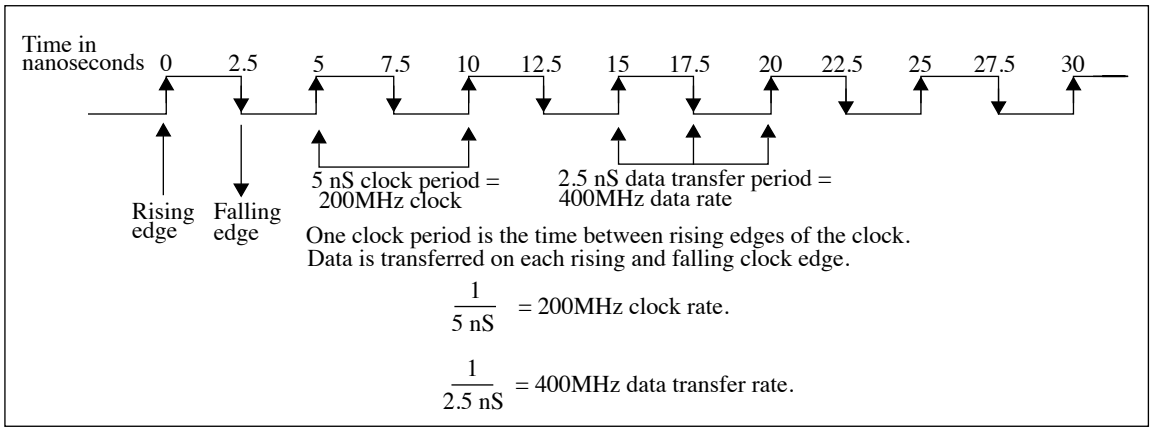


Figure 2.1 Attaining a 400MHz Data Rate

These unidirectional wires on each Crossbow ASIC device interface are not shared with any other devices in the system. This allows for a controlled electrical environment where the impedance of the traces is known and does not fluctuate. There is one driver and one receiver. Having dedicated connections allows for the preservation of signal integrity via tight control of transmission line effects and the minimization of clock skew. The mechanism used for these dedicated connections is called ‘low-voltage-swing signalling’ or STL (SGI Transistor Logic). Figure 2.2 shows a simple Crossbow connection diagram. The various devices represent those components in the system which interface to the Crossbow ASIC. These include the Heart ASIC, two Bridge ASICs, as well as graphics and expansion cards.

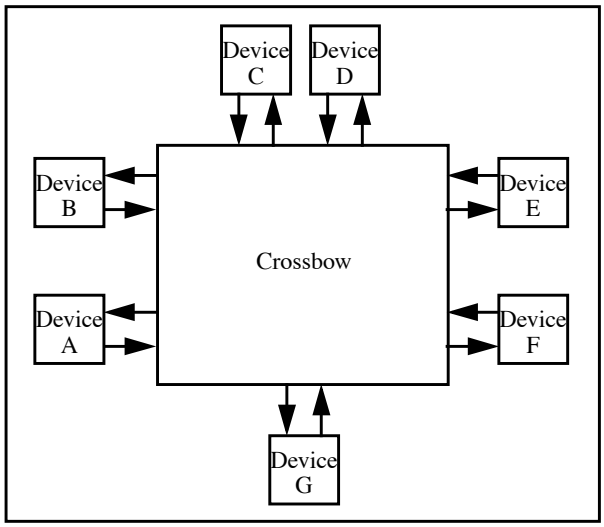


Figure 2.2 Crossbow Connection Diagram

The bandwidth problem is also solved through use of the Crossbow ASIC. The Crossbow acts a switch which connects every device in the system to every other device. Each device has a port which can communicate only with the Crossbow. The Crossbow in turn allows all of the devices to communicate with one another.

The Crossbow ASIC contains eight device ports. Seven ports are implemented on the OCTANE system as shown in Figure 2.2. Each port contains a dedicated 16-bit input and 16-bit output. With a 400MHz data rate, each port can operate at a peak bandwidth of 800MB per second in and 800MB per second out. Because these ports transfer information independent of one another, this allows for a maximum peak bandwidth of 1.6GB per second, which easily supports multiple streams of digital video.

### 2.1.2 OCTANE Board Layout

In order for the OCTANE system to support such high frequencies, parameters such as edge rates, transmission lines, characteristic impedance, signal reflections, and crosstalk, accorded little or no attention in lower-frequency systems, had to be tightly controlled during layout. In order for the OCTANE system to operate properly at these high frequencies, the following design issues had to be addressed:

- preservation of signal integrity by tight control of transmission line effects
- minimization of clock skew in the system
- mitigation of potential ground-bounce problems

At such high frequencies, every signal trace on the OCTANE system board has the ability to become a transmission line. An ideal transmission line is one where there is never any loss or distortion of the signal. Resistance in the signal trace is non-existent. The principle properties of a transmission line are its characteristic impedance and propagation delay per unit of

measure. Unfortunately, this ideal scenario does not exist. The fact is, transmission lines generate undesirable effects such as those listed above, creating an overall loss in both signal integrity and performance.

### 2.1.3 Packet Switching

The OCTANE system implements a packet-switched data transfer protocol for transferring data between the various devices in the system. This differs from the traditional "circuit-switched" protocol implemented in shared-bus architectures. In a circuit-switched protocol, once a connection between the two devices in the system has been established, no other ports on the system can talk to these devices. For example, once one of the peripheral devices has gained control of the bus to communicate with the CPU, none of the other peripherals in the system may use the bus to communicate with either the CPU or one another until the current transaction has completed.

In a packet-switched protocol, packets are defined as short bursts of information which are transferred between devices via a split-transaction protocol. The split-transaction protocol allows for multiple outstanding transactions on a given Crossbow link. The fundamental packet size is 128 bytes. Refer to Section 2.1.4 and Section 2.3.1.1 for more information on the packet-switched protocol.

### 2.1.4 Unfair Arbitration

A time slice is made up of a number of packet times. Figure 2.3 shows an example of a time slice containing 16 packets. Each letter represents a port on the Crossbow.

In Figure 2.3, the time slice is shown as 16 packet-times long. In this example, nine packets have been allocated to Device A, five packets to Device B, and two packets to Device C. Once a device has used its allocation, it must wait for the next time slice to send more data. For example, Device C was allotted two packets. Once the second packet is sent, Device C must wait for a new time slice before sending any subsequent packets.

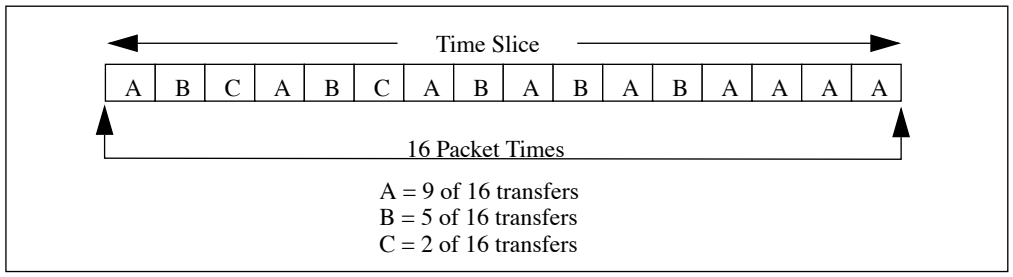


Figure 2.3 Packet-Switched Protocol

Devices A and B still have time left. Once Device B finishes its allocation, the remainder of the packets for this time slice can only be used by Device A. This is called "guaranteed unfair arbi-

tration" and allows streams to be prioritized. In the OCTANE system the most important streams from certain devices can be given priority over other devices. With one arbiter per port, the device priority in the OCTANE system is fully programmable.

### 2.1.5 Guaranteed Bandwidth and Latency

The Crossbow ASIC guarantees a worst-case average latency through support of a dual priority arbitration scheme. These dual arbiters are defined as the Guaranteed Bandwidth Ring (GBR) and the Remainder Ring (RR). A packet on the GBR, or high-priority bandwidth ring, will be transferred before a packet on the RR, or normal-priority ring. Each device is allowed to transfer a certain amount of packets per a given amount of time, as shown in Figure 2.3 above. The GBR ring is allowed to transfer one packet per time slice, whereas the RR ring is programmable from one to eight packets per time slice. This scheme defines a maximum number of packets which can be sent before a packet on the GBR is guaranteed to be transferred. This is called "Guaranteed Latency".

Devices on the GBR are allocated a given number of packets per time slice. The number of packets allowed by a given device per time interval is determined by the bandwidth counter which is set based on the types and priority of the transfers. A packet is eligible to participate in GBR arbitration if the corresponding GBR enable bit is set and the associated bandwidth counter (BWC) value is greater than zero. The BWC is decremented each time a request packet is transferred. When the BWC decrements to zero, that device falls from the GBR to the RR.

In Figure 2.3 for example, Device A is allocated 9 of 16 packets for the given time slice. However, there is no guarantee that Device A will use all 9 allocated packets. If this should occur, the remaining packets go to the RR. Therefore, if Devices B or C wish to send additional packets and they are available in the remainder ring, these two devices go through arbitration to determine which devices get which number of the remaining packets. The remainder ring is mostly used by devices which have not been allocated to the GBR.

Arbitration within the RR is done using a weighted arbitration scheme. Each device on the RR is allocated a number between one and eight. This value corresponds to the number of consecutive transfers allowed by that device before the RR arbiter grants the next requesting device.

The two-ring arbitration approach allows devices to be guaranteed a percentage of the available bandwidth taken from the GBR, and a distributed portion of the RR if more requests exist. Those devices that can tolerate latency in the transfer rate are not considered high-priority transfers, hence the corresponding bandwidth counter is set to zero and the device may only participate in the RR arbitration.

### 2.1.6 Data Transfer Types

Fundamental sizes for read requests are cache lines (128 bytes), quarter-cache lines (32 bytes), and doublewords (8 bytes).

A write request contains information regarding the target device, the fact that the cycle is a write, and how much data is being transferred. In the case of a write the response can be op-

tional. A ‘Fire and Forget’ write sends data and does not wait for a response from the target device verifying that the data has arrived.

If ordering is important, as is the case when multiple devices work on the same task and deliver the results to another device, a ‘Write-with-Response’ transfer protocol can be used. For example, Device A writes to Device B, and Device B returns a response. Device A then informs Device C that this transfer has completed successfully.

### 2.1.7 Link Level Protocol

The OCTANE system implements a ‘Link Level Protocol’ (LLP). This protocol consists of dedicated hardware which guarantees error-free delivery. In the LLP, the sending device breaks the data to be sent into 128-bit micropackets. Each micro-packet is tagged with a Cyclical Redundancy Check (CRC) value and a sequence number. The receiver checks the CRC value and acknowledges reception of the packet. If there is an error, the receiver logs the sequence number and asks the sender to retry that micro-packet. This is where the two links between the devices work well. Each CRC per micropacket is checked by the receiver. If a packet has an error, all subsequent packets in transit after the one that caused the error are ignored. The sender then re-sends the packet that caused the error. This packet is retried a programmed number of times. If data does not send correctly after the timer times out, an interrupt is generated.

This system is superior to both Error Checking and Correction (ECC) and parity. With ECC the error can be detected, but only single-bit errors can be corrected. With parity, a single-bit error can be detected but not corrected. The LLP protocol works even under severe conditions, such as when the links are operating at different speeds.

### 2.1.8 System Modularity

The OCTANE system decouples the processor and memory from the rest of the I/O subsystem. The processor interfaces to the Crossbow ASIC through the Heart ASIC, which connects to one of the Crossbow ports as shown in Figure 2.4. Note that there is no direct connection between the processor/memory system, and the I/O subsystem. Therefore, next generation processor or memory devices can be easily adapted without requiring changes to the I/O system. In addition, the OCTANE system supports both single- and dual-processor configurations. Figure 2.4 shows a block diagram of the OCTANE system.

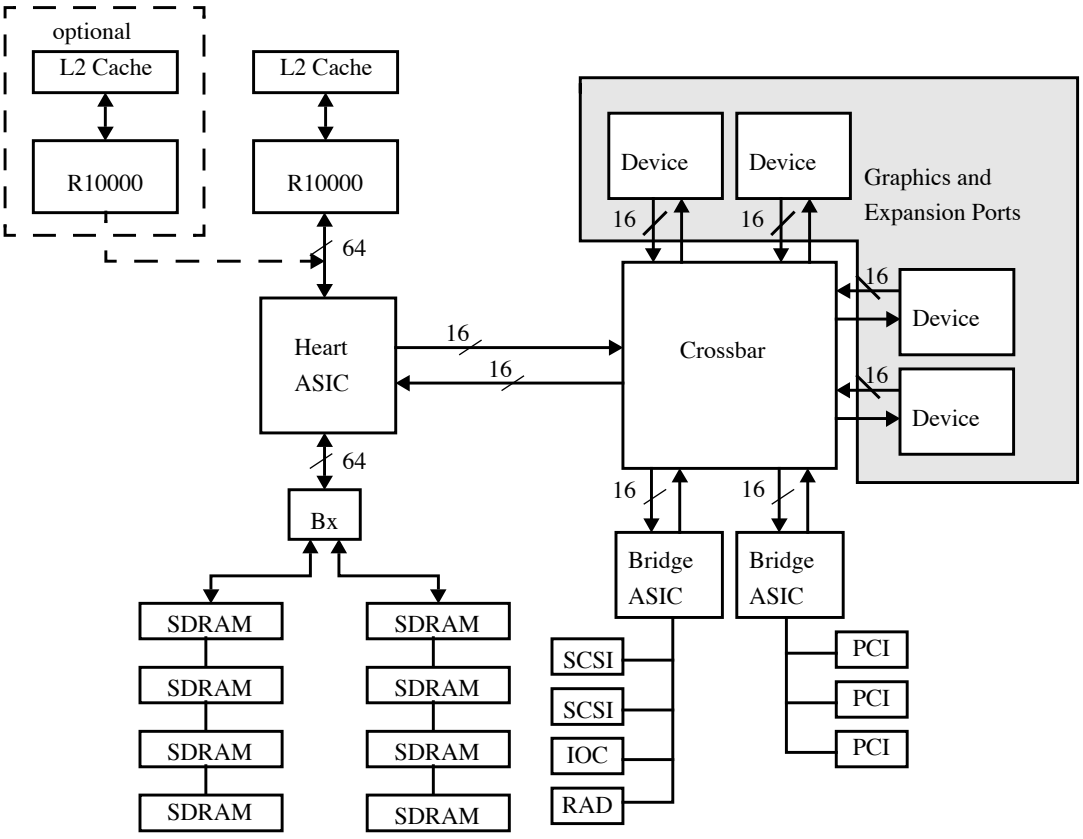


Figure 2.4 OCTANE System Block Diagram

As shown in Figure 2.4, the processor interfaces to one of the ports on the Crossbow ASIC through the Heart ASIC, which is the memory controller. The Bridge ASICs are used to interface various bus protocols such as SCSI and PCI to the Crossbow. The remaining four ports on the Crossbow are used for graphics and expansion cards.

### 2.2 R10000 Processor

The R10000 microprocessor is a 4-way super-scalar architecture which fetches and decodes four instructions per cycle. Instructions can be executed and completed out-of-order, meaning that it is not necessary to follow the original program sequence. The R10000 uses a technique called *Register Renaming* to keep instructions moving through the pipeline. Register renaming helps to alleviate the frequent stall conditions experienced by in-order machines due to dependencies between adjacent instructions.

Each decoded instruction is appended to one of three instruction queues. Each queue can perform dynamic scheduling of instructions. The queues determine the execution order based on the availability of the required execution units. Instructions are initially fetched and decoded in order, but can be executed and completed out of order, allowing the pipeline to have

up to 32 instructions in various stages of execution. The following sections explain some of the features of the R10000 processor.

### 2.2.1 Register Renaming

Dependencies between instructions often result in a stall condition and can degrade the performance of both the processor and the overall system. The R10000 processor uses *Register Renaming* to determine these dependencies. *Register Renaming* distinguishes between logical registers, which are referenced within the actual instruction, and physical registers, which are located in the hardware register file. The programmer is aware of only logical registers. The physical registers are hidden. Logical registers are dynamically mapped into physical register numbers using mapping tables which are updated after each instruction is decoded. Each new result is written into a physical register. In addition, the previous contents of each logical register are saved and can be restored in cases where the instruction must be aborted due to an incorrect branch prediction.

When a register is renamed the logical registers that are referenced in an instruction are mapped to physical registers using a mapping table. A logical register is mapped to a physical register whenever it becomes the destination of an instruction.

The instruction mapping scheme used to implement register renaming in the R10000 consists of a mapping table, an active list, and a free list. Separate mapping tables and free lists are provided for both integer and floating-point units. However, to maintain sequential ordering of instructions, only one active list exists that contains both integer and floating-point instructions. Figure 2.5 shows a block diagram of the instruction mapping scheme.

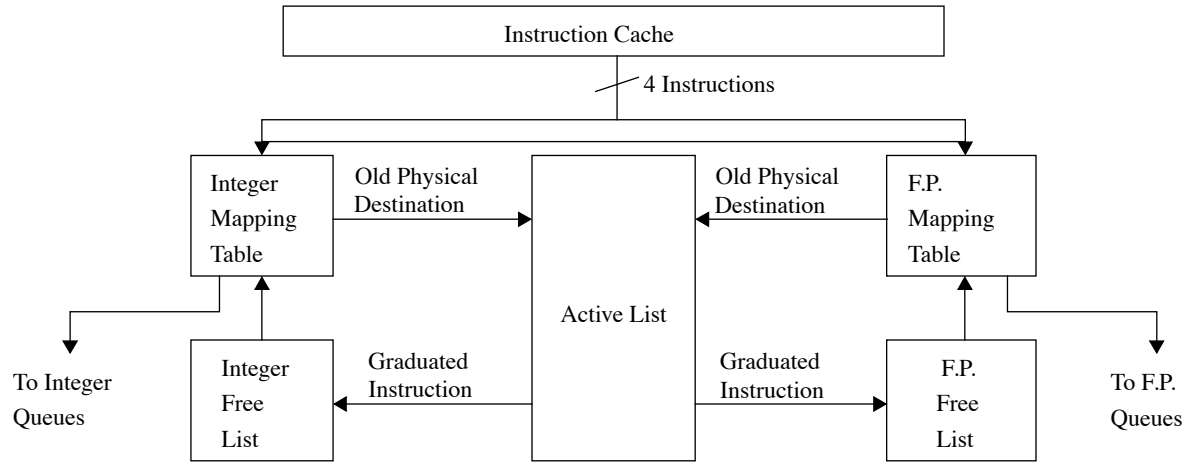


Figure 2.5 Instruction Mapping Scheme

The R10000 processor contains 64 physical registers. At any given time each of these 64 registers is contained in one of the lists shown in Figure 2.5. The active list maintains a listing of all 32 instructions in the pipeline at any given time. This list is always in-order.

### 2.2.2 Out-of-Order Execution

In a typical pipelined processor that executes instruction in-order, each instruction depends on the previous instructions which produced its operands. If the operands required to execute a given instruction are not valid, the pipeline stalls until they become valid. Because instructions are executed in-order in a typical pipelined processor, stalls usually delay all subsequent instructions.

The R10000 processor implements an out-of-order execution scheme. Each instruction is eligible to begin execution as soon as its operands become available, regardless of the original instruction sequence. Dedicated hardware effectively rearranges instructions in order to keep the various execution units busy. This process is called *dynamic issuing*. Instructions are fetched in-order four at a time, and can be executed and completed out-of-order. This type of execution scheme effectively eliminates the stall conditions experienced by in-order machines.

### 2.2.3 Non-Blocking Caches

In a typical microprocessor-based system, the processor executes out of the primary caches until a miss occurs. When a miss does occur, some number of cycles must elapse before data is fetched and placed in the primary cache, allowing execution to resume. This type of implementation is referred to as a *blocking cache* because the cache cannot be accessed again until the cache miss has been resolved.

The R10000 implements a non-blocking cache scheme which allows subsequent cache accesses to continue even though a cache miss has occurred. The R10000 supports up to four outstanding cache misses simultaneously. These cache misses can be resolved in any order. For example, if four cache misses are outstanding, and any one of these cache misses is resolved before a fifth cache miss is detected, the pipeline will never stall.

Locating cache misses as early as possible and performing the required steps to solve them is critical in increasing overall cache performance. The main advantage of a non-blocking cache is the ability to stack memory references by queueing up multiple cache misses and servicing them simultaneously.

### 2.2.4 Branch Prediction

As a general rule, branches interrupt pipeline flow and degrade overall performance. Branches occur frequently, approximately one out of every six instructions executed. The R10000 is defined as a 4-way superscalar processor, meaning that it can fetch four instruction per clocks. In the MIPS architecture, this means that a branch instruction can be encountered every other clock. Therefore, accurate branch prediction becomes very important for maintaining pipeline flow.

The branch unit can decode and execute one branch instruction per cycle. Since each branch is followed by a delay slot, the R10000 can fetch and decode a maximum of two branch

instructions simultaneously. A two-bit branch history RAM is used to determine the path of a predicted branch by keeping track of how often each particular branch was taken.

All instructions fetched after a branch instruction are speculative, meaning that it is not known at the time these instructions are fetched whether or not they will be completed. The R10000 processor allows up to four outstanding branch predictions which can be resolved in any order. A special branch stack maintains the information needed to restore the processor's state if the speculative branch is predicted incorrectly.

Figure 2.6 shows a block diagram of the R10000 processor. The following sections describe each block in the diagram.

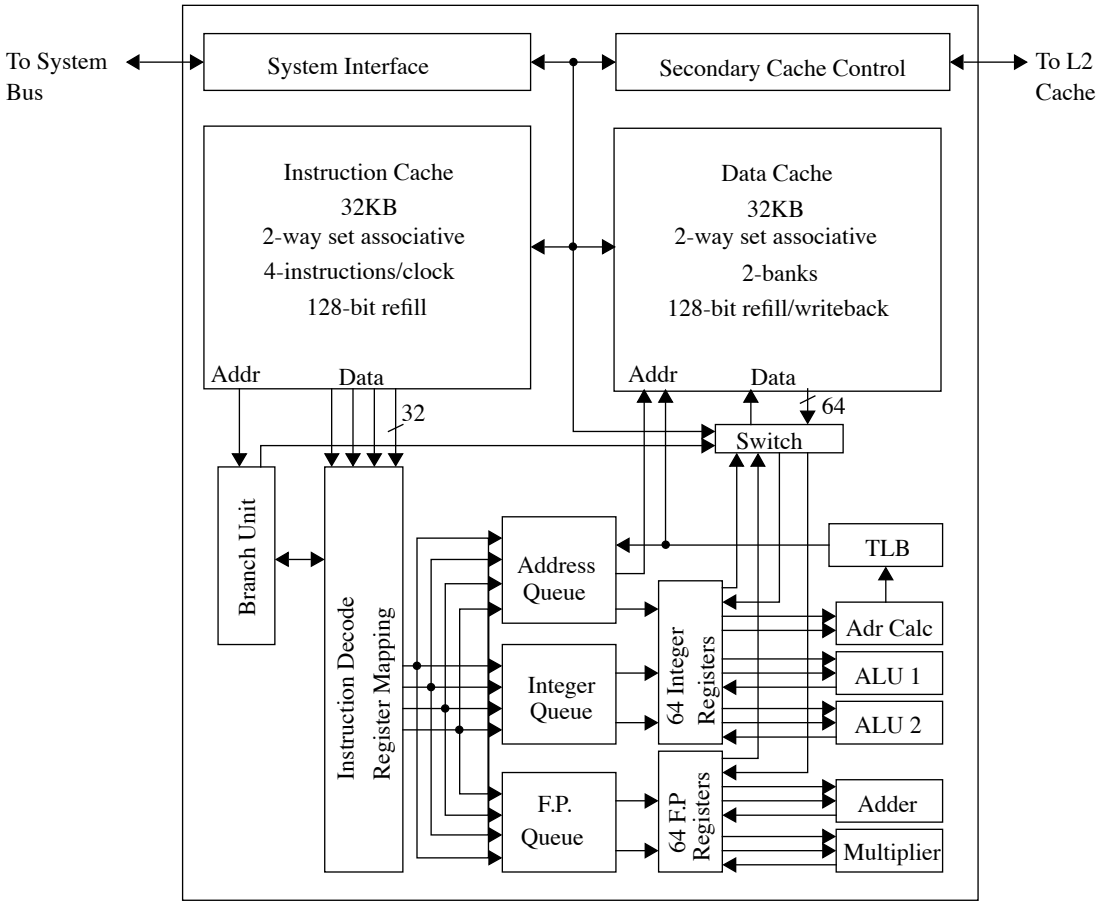


Figure 2.6 R10000 Processor Block Diagram

### 2.2.5 Primary Data Cache

The primary data cache is 32KB in size and is arranged as two identical 16KB banks. The cache is two-way interleaved, and each bank is two-way set associative. Cache line size is 32 bytes. The data cache is virtually indexed and physically tagged. Virtual indexing allows the cache to be indexed in the same clock in which the virtual address is generated. In a physically-indexed cache implementation, the cache cannot be accessed until the address goes through virtual to physical translation, resulting in at least a one-clock delay. Since only physical addresses are driven externally, the cache is physically tagged in order to maintain coherency with the secondary cache.

### 2.2.6 Primary Instruction Cache

The instruction cache is 32KB in size and is two-way set associative. Four instructions are fetched each cycle. Instructions are partially decoded before being placed in the instruction cache. Four extra bits are appended to each instruction to identify the execution unit to which the instruction will be dispatched. Instruction cache line size is 64 bytes.

### 2.2.7 Secondary Cache Interface

The secondary cache interface of the R10000 processor provides a dedicated 128-bit data bus which operates at the speed of the processor. The on-chip secondary cache controller generates all necessary synchronous static RAM (SSRAM) signals. No external interface circuitry is required. Minimum cache size is 512KB. Maximum cache size is 16MB. The secondary cache interface implements a split-transaction data transfer protocol and supports up to four outstanding secondary cache requests.

### 2.2.8 Instruction Queues

As shown in the Figure 2.6, the R10000 processor contains three instruction queues. These queues dynamically issue instructions to the various execution units. Each queue uses instruction tags to track instructions in each stage of execution.

The *Integer Queue* contains 16 entries and issues instructions to the two integer arithmetic logic units (ALU). Integer instructions are written into empty queue entries and up to four entries may be written each cycle. Integer instructions remain in the queue until being issued to an ALU.

The *Floating-Point* Queue contains 16 entries and issues instruction to the floating-point adder and floating-point multiplier execution units. Floating-point instructions are written into empty queue entries and up to four entries may be written each cycle. Instructions remain in the queue until being issued to the appropriate execution unit.

The *Address Queue* issues instructions to the Load-Store unit and contains 16 entries. The queue is organized as a circular FIFO (first-in first-out) buffer. Instructions can be issued in any order, but must be written to or removed from the queue in sequential order. The FIFO maintains the original program sequence so that memory address dependencies may be computed easily.

### 2.2.9 System Interface

The R10000 provides a 64-bit SysAD multiplexed address/data system interface bus which is completely separate from the 128-bit dedicated secondary cache interface. This bus is used to interface the system peripherals to the CPU. The clock speed is programmable between 50 and 195MHz. In the OCTANE system the peripheral devices interface to the system through the Crossbow ASIC. Therefore, the SysAD bus interfaces only to the Heart ASIC.

The system interface implements a split-transaction protocol. This protocol allows additional processor and external requests to be issued while waiting for a previous response. Each processor can have a maximum of four outstanding transactions on the bus at any time.

## 2.3 System ASICs

The majority of logic in the OCTANE system is implemented in three ASIC devices:

- *Crossbow*: Acts as the interface between the HEART ASIC and the I/O subsystem.
- *Heart*: Acts as the interface between the processor, memory array, and the Crossbow ASIC.
- *Bridge*: Acts as the interface between the Crossbow ASIC and the PCI bus peripherals.

### 2.3.1 Crossbow ASIC

The Crossbow ASIC is an 8 x 8 switch, meaning that there are eight ports and every port can communicate with every other port. In the OCTANE system, seven ports are implemented. Each port contains a 16-bit input and a 16-bit output. Each port can be programmed to be either 8- or 16-bits depending on the bandwidth requirements. Figure 2.7 shows a simple block diagram of the Crossbow ASIC.

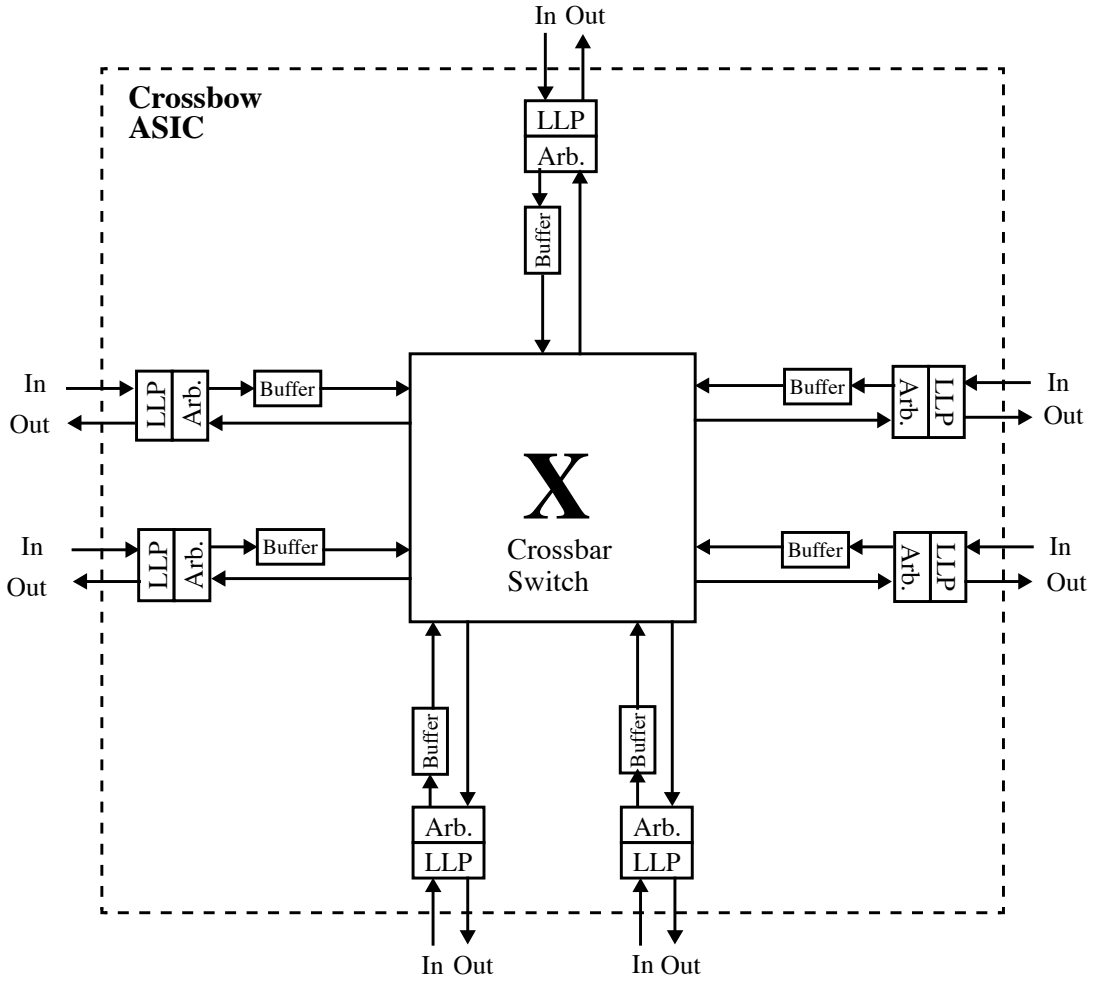


Figure 2.7 Crossbow ASIC Block Diagram

As shown in Figure 2.7, the Crossbow facilitates communication of devices having different data widths and also must accommodate different data rates. Equalization of data rates is accomplished by first storing the incoming packet into the input buffer where it is synchronized to the target data rate, then forwarded to the target. Conversely, during the response phase of the transfer, target data is stored into the input buffer on the Crossbow ASIC, synchronized, then forwarded to the source device. Buffer management is performed by the link level control logic.

The movement of packets through the Crossbow is done in two steps. The *Crossbow Link Flow Control* mechanism manages the transmission of data between the source device and the input buffer. The *Arbiter/Target Link Flow Control* mechanism manages the transfer of data between the input buffer, through the Crossbar switch, and on to the target device. Both of these flow control mechanisms are contained in the Crossbow ASIC.

The arbitration logic on each port of the Crossbow allows devices to talk to one another by defining the number of transfers which can occur at that port within a given time period. These finite time periods guarantee that any given device will be granted a connection to another device for the shortest possible time. In addition, the Crossbow allows multiple devices to communicate with one another simultaneously.

#### 2.3.1.1 Crossbow Packets

The Crossbow implements a packet-switched protocol and can facilitate simultaneous connections between the various devices in the system. Even after a connection between two devices has been established, packet-switching limits the amount of time that any given device can remain connected to any other device, allowing all peripherals in the system to have access to one another almost on demand.

The Crossbow supports eight basic types of packet transfers:

- Read Request
- Read Response
- Write Request
- Write Response
- Fetch and Operation
- Store and Operation
- Special Request
- Special Response

Packets are grouped into two types; *Request* packets and *Response* packets. Request packets are sent by the device which initiated the transaction. Response packets are sent by the target device as a reply to the request packet.

For each of the above transfers, the Crossbow supports three basic data transfer sizes; 8 bytes (doubleword), 32 bytes (quarter cache line), and 128 bytes (full cache line). The amount of data transferred depends on the type of transfer and the devices used.

The first four packet types above are used for basic communication between devices. The fetch and store packet types are used for memory operations. The special packet types allow two devices to define transfer lengths other than the three basic sizes. The total packet length must not exceed 140 bytes and must contain the command word.

#### 2.3.1.2 Packet Flow

A packet transfer consists of three phases; a *request phase*, an *operation phase*, and a *response phase*. During the request phase, the packet is moved through the Crossbow to the target device. The operational phase is where the target performs the requested function. During the response phase the target device sends a response back to the source as necessary. The response phase is not always required depending on the type of transfer. For example, on a ‘Fire-and-Forget’ write cycle explained in Section 2.1.6, Data Transfer Types, a response is not required. Figure 2.8 shows the flow of data during a packet transfer between two devices.

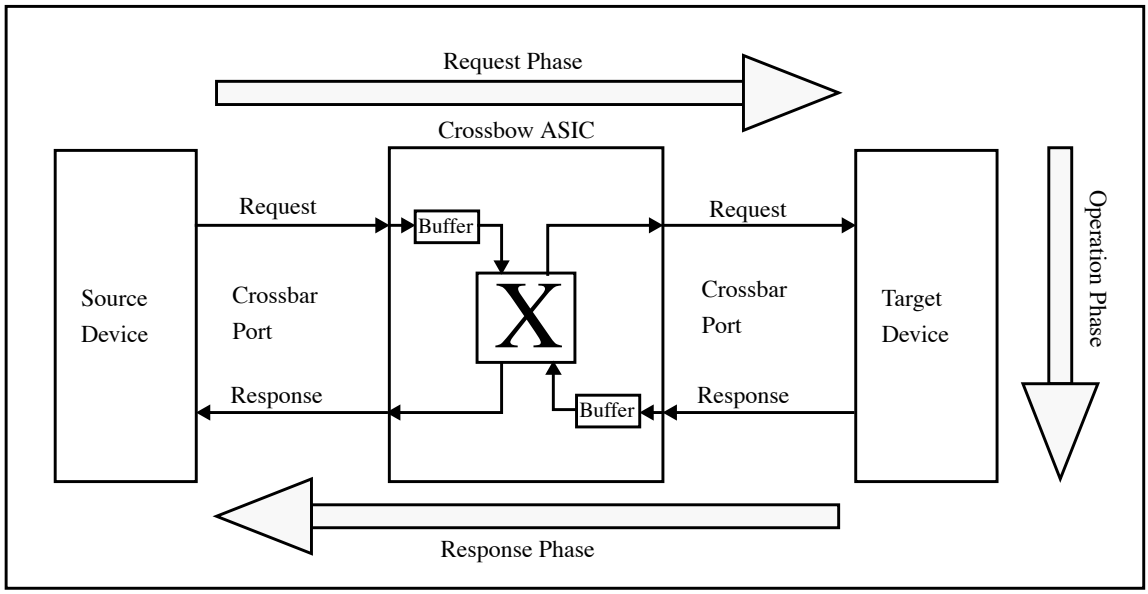


Figure 2.8 Packet Flow Diagram

### 2.3.2 Heart ASIC

The Heart ASIC provides the interface between the MIPS R10000 processor, external main memory, and the I/O subsystem attached to the Crossbow ASIC. As shown in Figure 2.4, the Heart ASIC connects to one of the ports on the Crossbow ASIC and allows the processor and main memory to be decoupled from the rest of the I/O subsystem. This decoupling allows for easy upgrades to faster processors or memory subsystems without having to re-design the entire system board.

The Heart ASIC manages the flow of data for the following six data transactions.

- Processor to memory read.
- Processor to memory write.
- Processor to I/O subsystem read.
- Processor to I/O subsystem write.
- I/O subsystem to memory read.
- I/O subsystem to memory write.

Figure 2.9 shows a simplified block diagram of the Heart ASIC which focuses on the flow of data between the major interface units. The following sections explain each interface block.

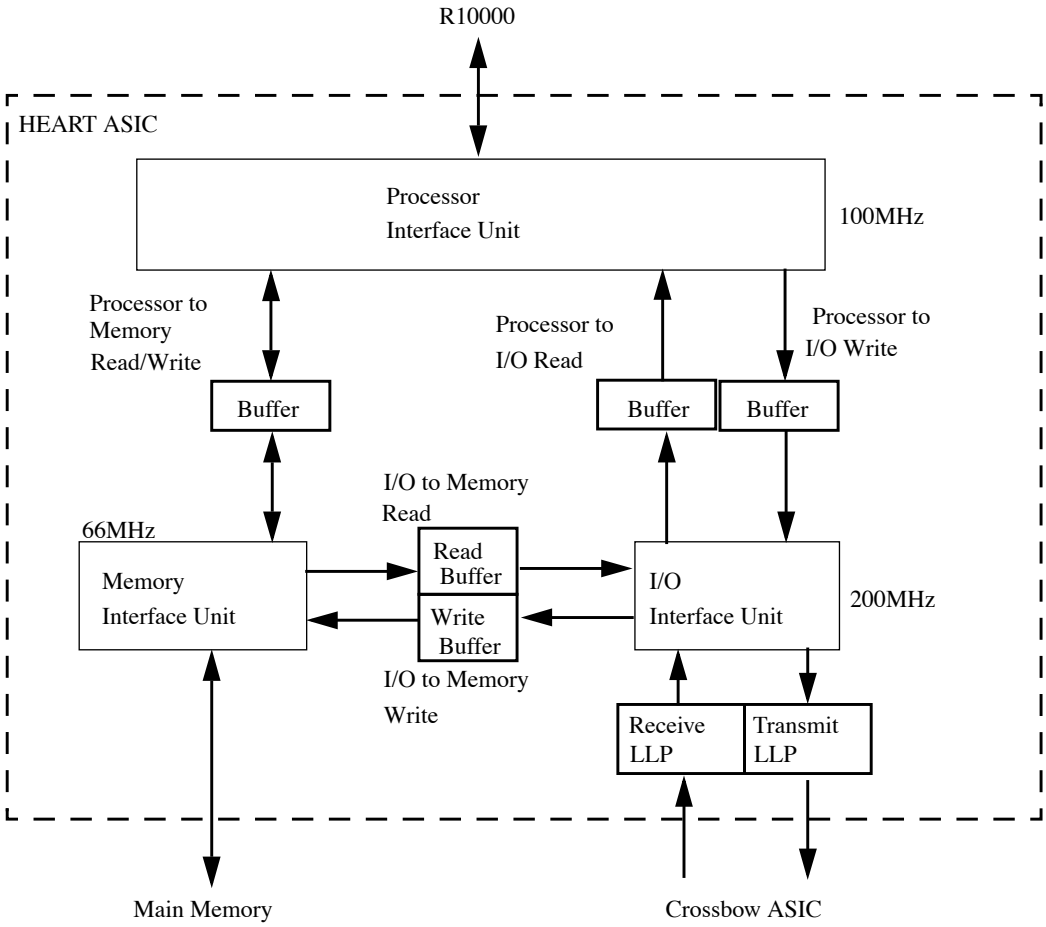


Figure 2.9 HEART ASIC Simplified Block Diagram

#### 2.3.2.1 Processor Interface Unit

The *Processor Interface Unit* (PIU) acts as the external agent for the R10000 processor and arbitrates for ownership of the R10000 SysAD multiplexed address/data bus. In addition, the Heart ASIC manages I/O requests for both the memory subsystem and the processor. The Heart ASIC arbitrates its hardware resources for both I/O and processor requests to provide a real-time guaranteed response to the I/O subsystem and to avoid dead-lock conditions.

The PIU interfaces to the *Memory Interface Unit* and *I/O Interface Unit* through dedicated data buffers shown in Figure 2.9. Because each of these interface units operates at different speeds, these buffers provide an asynchronous boundary between the various units. The PIU operates at the processor bus clock frequency and supports a maximum frequency of 100MHz.

The Heart ASIC supports both single- and dual-processor configurations without the need for any additional external logic. During reset, the Heart ASIC determines the number of

processors and programs the PIU accordingly. Each processor contains dedicated grant and request signals as well as processor state signals which connect directly to the Heart ASIC. These signals allow the Heart ASIC to determine the master/slave and processor state status of each processor and arbitrate the SysAD bus between processors.

#### 2.3.2.2 Memory Interface Unit

The *Memory Interface Unit* (MIU) controls the SDRAM-based main memory subsystem and generates all main memory cycles. The MIU receives requests for memory accesses from both the PIU and the *I/O Interface Unit*. The MIU arbitrates these memory accesses in order to provide a real-time I/O response guarantee which maximizes I/O subsystem throughput.

The MIU operates at 66MHz. To minimize pin count on the Heart ASIC, this frequency is doubled to 133MHz at the memory interface pins. After the data reaches the memory data buffers, the frequency is divided back down to 66MHz. The main memory system is implemented using Synchronous DRAM (SDRAM) devices.

Memory requests from I/O devices through the Crossbow ASIC can be arbitrated on either the *Guaranteed Bandwidth Ring* (GBR) or the *Remainder Ring* (RR). Each of these rings is defined at the beginning of this section. The GBR always has priority over the RR. In general, the memory access priority is as follows:

- I/O to memory accesses on the GBR.
- Processor to memory read accesses.
- I/O to memory accesses on the RR.
- Processor to memory write accesses.

#### 2.3.2.3 I/O Interface Unit

The *I/O Interface Unit* (IOU) connects to one of the ports on the Crossbow ASIC and provides the interface between the processor and the I/O subsystem. The IOU communicates to the Crossbow ASIC through two 16-bit unidirectional links running at 400MHz. These two links operate independently of one another. The IOU generates request packets to the Crossbow ASIC during processor to I/O read and write operations. During read accesses, the read data is sent to the PIU via the read data buffer. During write requests, processor data is sent to the IOU and out to the Crossbow port through the write data buffer.

The IOU also receives I/O-to-memory read and write requests. The IOU transfers data between the Crossbow port and the MIU through a set of unidirectional data buffers. The MIU reads I/O requests out of a dedicated I/O request buffer, where the IOU stores the requests in order. During these types of requests, the PIU monitors the type and location of the I/O-to-memory operation in order to maintain data coherency between the processor caches and main memory. In the OCTANE system, the contents of the primary cache inside the R10000 are always a subset of the secondary cache, and the contents of the secondary cache are always a subset of what is in main memory. Therefore, if the I/O subsystem desires to write to a main memory location which also resides in one of the caches, the processor must be aware of this operation and update its caches accordingly to insure data coherency. The IOU cannot access the processor caches directly. The IOU uses a 200MHz clock and transfers data to and from the Crossbow ASIC on both edges of this clock, creating a 400MHz data rate.

#### 2.3.2.4 Transmit and Receive LLP

The Transmit and Receive LLP blocks perform the *Link Level Protocol Interface* to the respective input and output ports of the Crossbow ASIC. As discussed in Section 2.1.7, the LLP protocol consists of dedicated hardware which guarantees error-free delivery and is superior to both Error Checking and Correction (ECC) and parity data verification schemes.

#### 2.3.2.5 Data Integrity

The Heart ASIC interfaces to various devices which implement different types of data integrity protocols. The Heart ASIC uses the Cyclical Redundancy Check (CRC) data integrity protocol when transferring data to and from the Crossbow ASIC. The processor and memory interfaces utilize the ECC protocol. I/O operations to the PCI bus implement a parity protocol. Figure 2.10 shows how the various data integrity protocols are implemented throughout the system.

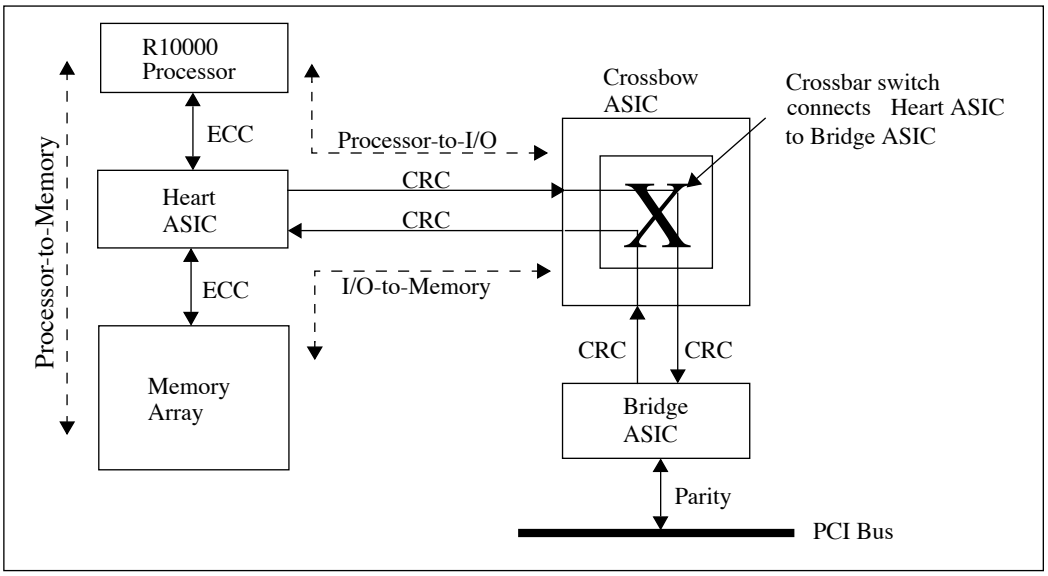


Figure 2.10 OCTANE Data Coherency Schemes

During processor-to-memory cycles, the processor attaches ECC check bits to the doubleword of data being transferred. The MIU in turn passes these bits onto the memory array.

During a *processor-to-I/O write* cycle, the data integrity protocol must be modified during the transfer in order to maintain compatibility with the various devices. The protocols are modified as follows:

- The processor attaches ECC check bits to the data, which is then driven to the Heart ASIC.
- The Heart ASIC checks the ECC bits. If there was no error during the transfer, the Heart ASIC drops the ECC bits and attaches CRC check bits. This data packet is then passed to the Crossbow ASIC.

- The Crossbow ASIC connects the Heart ASIC to the Bridge ASIC through the internal Crossbar switch. Refer to Figure 2.10. The Bridge ASIC checks the CRC check bits. If there was no error during the transfer, the Bridge ASIC drops the CRC check bits and attaches parity bits to the data.
- The data with parity attached is then passed to the appropriate PCI device.

During a *processor-to-I/O read* cycle, data is transferred in the reverse order. The Bridge ASIC receives data from the PCI device and checks the parity bit. If there is no error, the Bridge ASIC drops the parity and attaches CRC check bits for transfer to the Crossbow ASIC. Once this data arrives at the Heart ASIC, the CRC check bits are checked and then dropped and ECC bits are attached. The data with ECC attached is then passed to the processor.

*I/O-to-memory read* cycles are handled almost the same as the processor-to-I/O write cycle discussed above. The requesting I/O device initiates a memory read. Memory data is fetched with ECC bits attached. The Heart ASIC checks and then drops the ECC bits and generates CRC check bits for transfer to the Bridge ASIC. The Bridge ASIC in turn checks and then drops the CRC check bits and attaches parity. The data is then sent to the requesting PCI device with the correct data integrity protocol attached.

During *I/O-to-memory write* cycles, data is transferred in reverse order as an I/O-to-memory read. The Bridge ASIC receives data from the appropriate device, checks and then drops the parity, and attaches CRC check bits. Once this data arrives at the Heart ASIC, the CRC check bits are checked and then dropped and ECC bits are attached. The data with ECC attached is then stored in the memory array.

### 2.3.3 Bridge ASIC

The two Bridge ASICs in the OCTANE system provide bus protocol conversion between the Crossbow device and the industry standard PCI bus. One Bridge ASIC supports built-in peripherals such as SCSI, Ethernet, audio, serial ports, and parallel ports. The second Bridge ASIC provides an interface to four PCI bus slots which can be used for add-on cards. The Bridge ASIC provides support for address mapping, interrupt control, and prefetching of data. Separate transmit and receive logic allows the Bridge ASIC to both transmit data to the Crossbow and receive data from the Crossbow at the same time. Figure 2.11 shows a simplified block diagram of the Bridge ASIC.

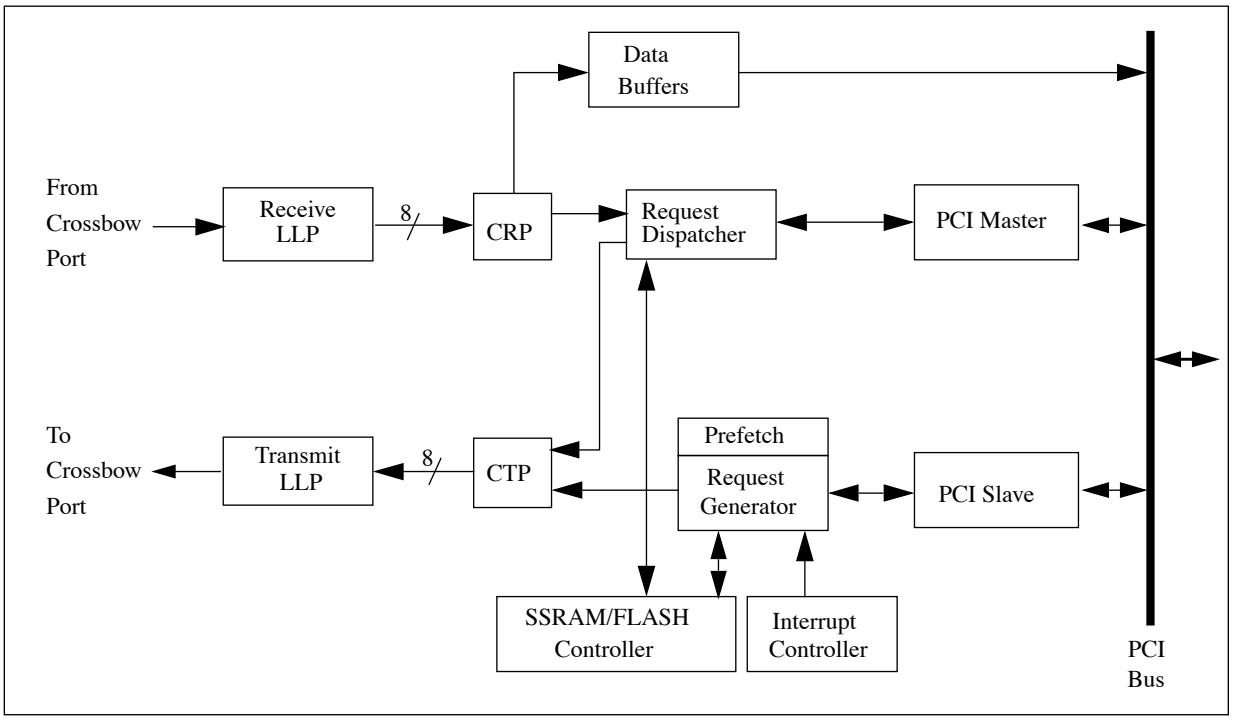


Figure 2.11 Bridge ASIC Block Diagram

#### 2.3.3.1 Transmit and Receive LLP

The Transmit and Receive LLP blocks perform the *Link Level Protocol Interface* to the respective input and output ports of the Crossbow ASIC. As discussed in Section 2.1.7, the LLP protocol consists of dedicated hardware which guarantees error-free delivery by attaching CRC check bits to the data. The CRC data integrity protocol is superior to both Error Checking and Correction (ECC) and parity data integrity protocols.

#### 2.3.3.2 Transmit and Receive Processors (CTP/CRP)

The *Crossbow Transmit Processor* (CTP) and *Crossbow Receive Processor* (CRP) are used to interface the Bridge ASIC to the Crossbow port. These two communications processors are programmed to be eight bits wide and operate independently of one another. The CRP receives data packets from the Crossbow ASIC and transfers them to either the data buffers or the request dispatcher. The CTP gathers responses and bus-generated requests and transfers them to the Crossbow ASIC.

#### 2.3.3.3 Request Dispatcher

The *Request Dispatcher* decodes and distributes all incoming requests to the various functional units. In addition, the *Request Dispatcher* is responsible for returning a response from those requests, while providing any necessary address translation and error checking.

#### 2.3.3.4 Request Generator

The *Request Generator* is responsible for request packet generation, address translation, and response buffer management. To enhance read access performance, the Bridge ASIC supports prefetching of data which allows for faster read response times when sequential read cycles are performed by devices on the PCI bus.

#### 2.3.3.5 Data Buffers

The data buffers shown in Figure 2.11 provide a mechanism for buffering data between the Crossbow ASIC and the devices on the PCI bus. Data buffering is necessary due to the differences in speed and bandwidth between the OCTANE system and PCI peripheral devices. Data written from the high-speed Crossbow ASIC can be stored in the data buffer, then synchronized and transferred to the lower-speed PCI bus. Without these data buffers, the Crossbow ASIC would effectively have to enter a stall condition, continually driving data through the Bridge ASIC until it is received and stored by the PCI peripheral. The data buffers are also used to hold the prefetched data for PCI read requests.

#### 2.3.3.6 PCI Bus (Master and Slave)

The PCI local bus supports both 32- or 64-bit wide devices and contains multiplexed address and data busses. PCI is a synchronous bus which can operate at up to 33MHz, resulting in a reasonably high data transfer rate. Peripheral devices on the PCI bus can act as a bus master, transferring data to and from the OCTANE system. In addition, a given peripheral device can access other devices on the PCI bus.

The incorporation of the PCI bus into the OCTANE system allows Silicon Graphics customers access to high performance, low cost, third party peripheral devices which can be interfaced directly to the OCTANE system. For example, the baseline audio system in the OCTANE provides 8 channels of 24-bit audio, but supports up to 32 channels which could be added via PCI add-in cards.

#### 2.3.3.7 SSRAM/FLASH Interface

The SSRAM/FLASH controller supports local SSRAM for storage of address translation entries and a FLASH ROM for boot support. The controller supports the following SSRAM configurations:

The Bridge ASIC provides a dedicated SSRAM/FLASH interface which is not accessible from the PCI bus. The controller supports FLASH ROM configurations up to 2M x 16. The FLASH ROM is used as the boot PROM

## 2.4 Memory System

The main memory system interfaces to the Heart ASIC through special high-speed data and address buffers. The interface between the Heart ASIC and the buffers operates at 133MHz, whereas the interface between the buffers and the SDRAM array operates at 66MHz. Figure 2.12 shows a block diagram of the main memory subsystem.

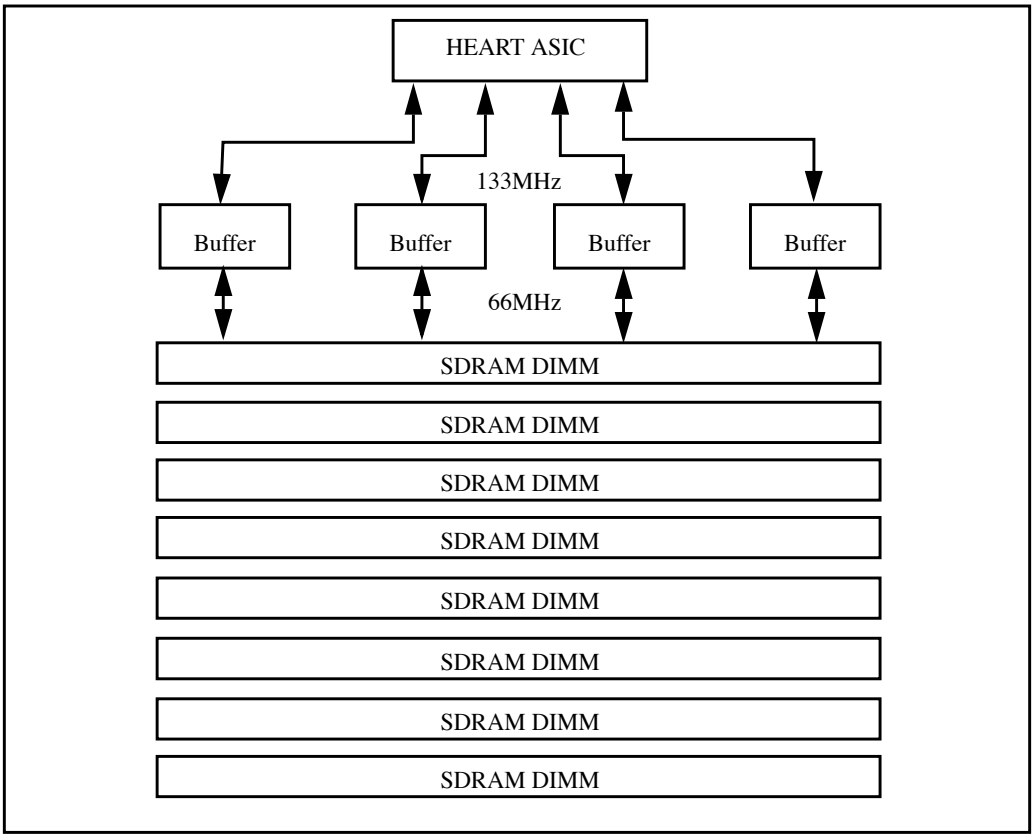


Figure 2.12 Main Memory Subsystem

The OCTANE memory interface offers a high level of flexibility when configuring the memory system. The memory system ranges from 16MB to 2GB in size and can accommodate multiple sizes of single-bank or dual-bank *Dual-bank In Line Memory Modules* (DIMMs). The OCTANE memory system allows the user to mix different sizes of DIMMs in order to customize their memory system. In addition, the OCTANE system incorporates the industry standard 72-pin DIMM connector pinout, allowing the user to add off-the-shelf memory devices. Table 2.1 shows the memory devices supported.

Table 2.1 DIMM Configurations

| DIMM Configuration | Number of Banks | Memory Configuration | Size per SIMM | Size per DIMM Bank |
|---|---|---|---|---|
| Single-Bank DIMMs | | | | |
| 4M x 72 | 1 | (1) (4M x 4) x 18 | 32MB | 64MB |
| 8M x 72 | 1 | (1) (8M x 8) x 9 or<br>(1) (8M x 9) x 8 | 64MB | 128MB |
| Dual-Bank DIMMs | | | | |
| 8M x 72 | 2 | (2) (4M x 4) x 18 | 64MB | 128MB |
| 16M x 72 | 2 | (2) (8M x 8) x 9 or<br>(2) (8M x 9) x 8 | 128MB | 256MB |
| 32M x 72 | 2 | (2) (16M x 4) x 18 | 256MB | 512MB |

### 2.4.1 Synchronous DRAMs

The Synchronous Dynamic RAM (SDRAM) represents the next step in the evolution of the industry standard DRAM architecture. While there are many similarities between DRAMs and SDRAMs, there are also many differences which allow SDRAMs to enhance system throughput and overall memory system performance. The clocked, multi-bank architecture of the SDRAM supports far greater data rates than are available with standard DRAMs.

The most significant performance advantage that SDRAMs have over standard DRAMs is the ability to pipeline internal accesses. In a standard DRAM, the toggling of the external pins has a direct effect on the internal memory array. In an SDRAM, the toggling of the external pins causes transitions in an internal state machine. These transitions in turn control the actual memory access. This approach allows for pipelining of accesses in an SDRAM, whereas with the standard DRAM pipelining of accesses is not possible.

In an SDRAM, all control signals are sampled on the rising edge of a clock. Therefore, these control signals need only be asserted for one clock, meaning that the processor need only drive address and control signals for as long as it takes for this information to be recognized by the SDRAM controller. Not having to drive address and control signals throughout the entire memory cycle, as is necessary with standard DRAMs, greatly enhances the systems ability to pipeline memory cycles and allows data to be driven by the SDRAM on every clock. Figure 2.13 shows the difference between the pipelines of an SDRAM and a standard DRAM during a 5 clock period. In the SDRAM pipeline, data from address 1 is output in clock 4, and data from address 2 is output in clock 5. Note that once the pipeline is full as shown in clock 4, data can be output every clock. By contrast, a standard DRAM architecture has asynchronous control signals and cannot pipeline addresses. The address must remain valid throughout the entire memory cycle until data is output. In this example a standard DRAM can output data only on every fourth clock.

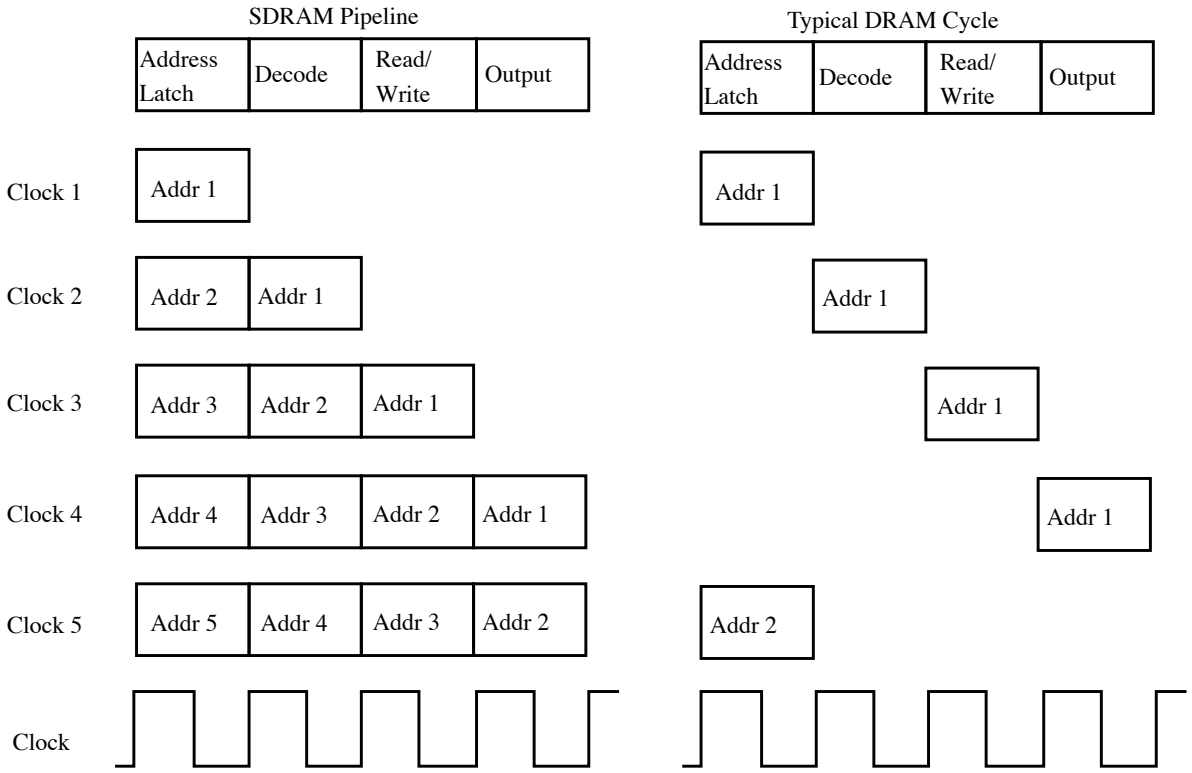


Figure 2.13 SDRAM Pipeline

In addition to the pipeline, the SDRAM also incorporates a split-bank architecture which effectively mimics a two-way interleaved memory system without the need for two separate physical banks. Each bank can operate independently of one another. Once a given row of a given bank has been accessed, it can be held active and accessed on every clock by simply supplying a new column address.

The programmability of the SDRAM allows it to be customized to each OCTANE system. Parameters such as Column Address Select (CAS) latency and burst length can be defined in the on-chip Mode register.

### 2.4.2 Memory Data Integrity

The memory array in the OCTANE system uses a data integrity scheme called *Error Checking and Correction* (ECC). The MIU in the Heart ASIC generates ECC check bits for every double word from either processor of I/O devices.

### 2.5 I/O Subsystem

The OCTANE I/O subsystem consists of the following interfaces:

- SCSI
- Keyboard and Mouse
- Ethernet
- Serial Ports
- Parallel Port
- Audio

With the exception of the SCSI interface which is managed by a dedicated SCSI controller, and the audio interface (discussed in Section 3) which is managed by the RAD ASIC , each of the above I/O interfaces is controlled by the IOC3 ASIC. This ASIC was designed by Silicon Graphics and connects to the OCTANE system board via a 32-bit PCI interface. Figure 2.14 shows the function of the IOC3 ASIC. Note that all of the blocks shown are contained on the OCTANE system board.

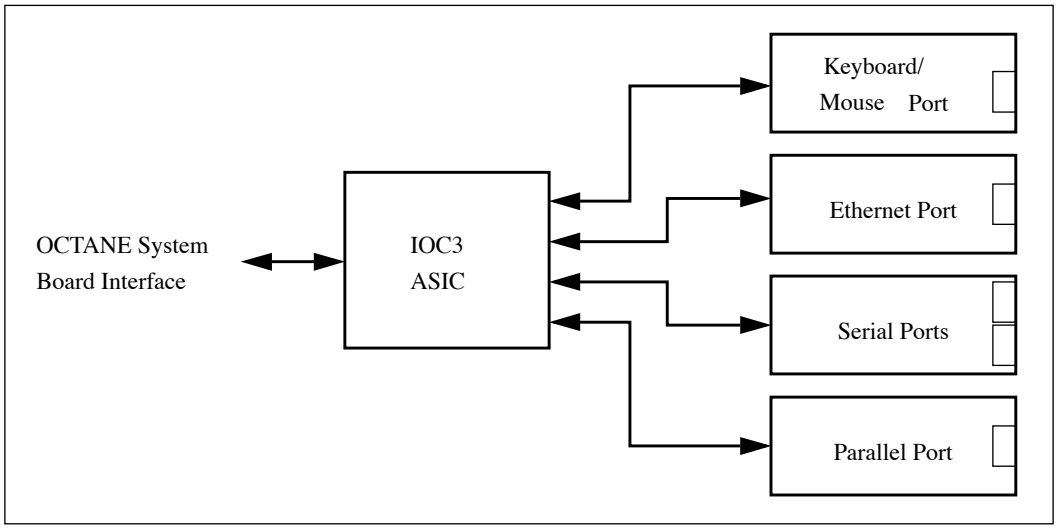


Figure 2.14 IOC3 ASIC Interface

The IOC3 ASIC manages the flow of data from the keyboard and mouse and acts as the interface between the keyboard/mouse and the OCTANE system board. The OCTANE implements the industry-standard PS/2 style keyboard and mouse interface.

The IOC3 ASIC contains an integrated 10/100 MBit Ethernet Media Access Controller (MAC), a highly optimized DMA buffer management mechanism, and the control logic for a store-and-forward buffer contained in an external SSRAM. The DMA structure is designed to minimize programmed I/O transfers, interrupts, and cache misses in the Ethernet driver. The store-and-forward buffer is provided so that periods of high system memory latency can be

tolerated. This buffer allows the OCTANE system to achieve a sustained 100Mbits per second data rate. The IOC3 ASIC connects to a separate 10/100Base-TX Ethernet PHY that is located on the OCTANE system board.

### 2.5.1 SCSI Interface

To enhance overall performance, the SCSI interface consists of two busses; internal, and external. These two busses are logically identical. Having two busses increases performance and simplifies system peripheral configurations that commonly arise with a single bus. The *internal* bus is completely separate from the external bus and is dedicated to the three internal drive bays in the OCTANE system. The *external* bus is managed by a SCSI controller and supports up to fifteen external SCSI devices. The external bus allows devices to be installed and configured without affecting the operation of performance or the internal drives.

#### 2.5.1.1 Internal SCSI Bus

The Internal SCSI bus mechanism contains four sections;

- SCSI Controller
- Frontplane Bus
- SCSI Extender
- SCSI backplane

Figure 2.15 shows the flow of data between the OCTANE system board and the internal SCSI bus.

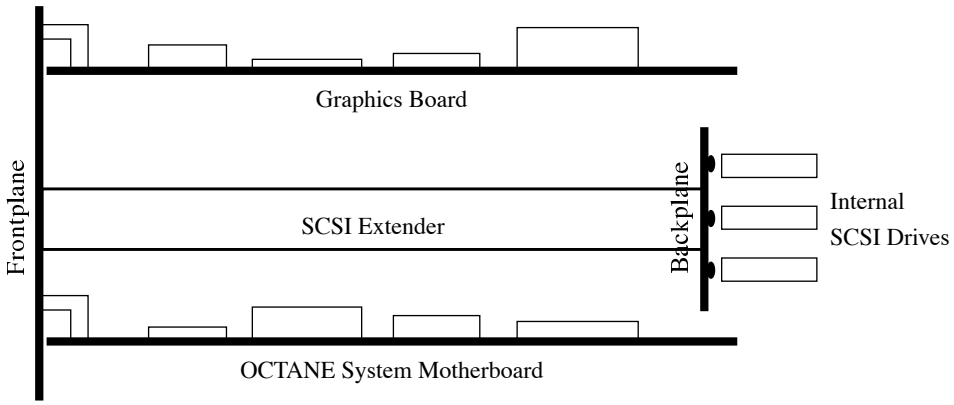


Figure 2.15 Internal SCSI bus Data Flow

The signal path for SCSI transfers to the internal bus is as follows:

OCTANE Motherboard → Frontplane → SCSI Extender → Backplane

**SCSI Controller** - The internal SCSI bus is driven by a dedicated SCSI controller connected to the PCI bus on the OCTANE system board. The controller supports both Fast (10MHz) and Ultra (20MHz) SCSI timing. Both Wide (16-bit) and Narrow (8-bit) devices are also supported, allowing for a maximum bandwidth of up to 40MB per second. The controller manages the DMA transfer of descriptor blocks from memory, executes these blocks, and initiates the DMA transfer of the resulting data to and from the address specified in the descriptor block. The controller uses an external SRAM to store descriptor blocks as well as its own microcode. The internal SCSI bus is terminated at the controller and on the SCSI backplane using active termination.

**Frontplane** - As shown in Figure 2.15, the frontplane is a printed circuit board (PCB) that each of the OCTANE system boards plug in to. The frontplane facilitates the physical connection between each of the system boards and allows them to communicate with one another. To insure signal integrity on the frontplane, the SCSI bus is routed away from the 400MHz unidirectional links which connect the various devices in the system to the Crossbow ASIC on the system motherboard. The SCSI traces maintain a constant 90 Ω characteristic impedance.

**SCSI Extender** - A simple 6-layer PCB is used to connect the frontplane to the SCSI backplane. The OCTANE system uses low-profile pin headers and sockets to facilitate the connection at each end. This proved to be the simplest and most cost-effective approach to maintaining the 90 Ω characteristic impedance versus cables of flexible wires.

**SCSI Backplane** - The SCSI backplane consists of a 6-layer PCB containing 3 connectors for the internal SCSI drives. The OCTANE system board contains active termination at the end of the SCSI bus in order to maintain the characteristic 90 Ω impedance.

#### 2.5.1.2 External SCSI Bus

The *external* SCSI bus is similar to the internal SCSI bus. The *external* bus is managed by a SCSI controller and supports up to fifteen SCSI devices. The *external* bus allows devices to be installed and configured without affecting the operation of performance of the internal drives. Active termination is required if the device is on the external bus.

### 2.5.2 Keyboard and Mouse

The OCTANE system provides a PS/2-compatible keyboard and mouse interface. The interface is managed by the IOC3 ASIC and provides for independent receive data packing for the two ports and single character writes to each. The receive data packing mechanism is a performance optimization designed to reduce the load on the R10000 CPU.

There is an external buffer between the inputs of the keyboard/mouse connector and the IOC3 ASIC, and another between the IOC3 output pins and the keyboard/mouse connector. These buffers provide higher drive capability and better isolation for electro-static discharge (ESD).

The maximum recommended distance of the keyboard and mouse from the OCTANE system is limited to approximately 10-15 feet.

### 2.5.3 Ethernet Interface

The OCTANE system supports a 10/100MBit Ethernet port. The port can be configured to operate in either 10Base-T or 100Base-TX transfer formats. On-chip hardware detects which format is in use and auto-configures the device. The Ethernet interface is implemented using the IOC3 ASIC, a buffer SSRAM, and an off-the-shelf PHY transceiver chip.

### 2.5.4 Serial Port Interface

The serial port interface is implemented using the IOC3 ASIC. The ASIC functions as the interface between the PCI bus and an off-the-shelf serial/parallel port device which contains two 16550-compatible Universal Asynchronous Receiver/Transmitter (UART) serial ports and an IEEE-1284-compatible parallel port.

The serial port baud rates are programmable between 300 to 460KBaud. The two serial ports can either be accessed directly with Programmable I/O (PIO) operations, or by using the ring buffers in host memory in order to reduce the number of both interrupts and PIO operations. The 16550-compatible serial ports support the following baud rates:

- 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200, 9600, 19200, 31250, 38400, 56000, 115200, 230400, 460800

The serial port electrical interface can be programmed to operate in either of the following modes:

- PC-compatible RS-232 interface level
- Macintosh style interface level

Most general purpose serial port peripherals use the RS-232 interface. The Macintosh mode is provided to enable two main types of applications:

- MIDI interface using a Mac-to-MIDI adapter
- Digital media machine control which conforms to the SMPTE 207M standard

### 2.5.5 Parallel Port Interface

The parallel port is an IEEE 1284-compliant unidirectional port for connecting printers and other devices. The parallel port is located in the serial/parallel device discussed in Section 2.5.4. The parallel port interface is implemented using the IOC3 ASIC. The IOC3 provides DMA support for the parallel port FIFO-compatibility mode. To enhance the performance of DMA transfers, the IOC3 ASIC supports two contexts which allow one buffer in host memory to be transferred while the next buffer is being prepared for transfer.

# *Section 3 Audio Architecture*

## 3.1 Audio System

Supporting user environments that range from routine personal desktop sound to the most demanding professional applications, OCTANE provides a scalable, synchronizable audio architecture. Native features include analog stereo I/O, coaxial digital stereo I/O (AES3), ADAT Optical interface 8-channel I/O, and a synchronizable infrastructure suitable for high-end professional audio and video post-production.

For software developers, the Audio Library (AL) application programming interface provides a standard programming environment which spans the entire SGI product line. Using the AL, developers can utilize the full functionality of the newest professional audio configurations. Some of the more notable professional application areas include:

- sound synthesis and editing for entertainment media
- subjective sound engineering/analysis for industrial products
- speech analysis and research
- environmental simulation

Each OCTANE system offers a complete set of personal sound I/O capabilities. This includes a mono microphone (with noise gate and limiter) and workstation-powered stereo desktop speakers. Using the microphone, users can easily add voice annotation to multimedia documents and participate in teleconferencing applications. The desktop stereo loudspeakers provide the complimentary function, allowing users to listen to any applications that provide sound output. The loudspeakers also provide a convenient stereo headphone connection.

The OCTANE baseline audio system incorporates the RAD ASIC, which interfaces to analog stereo I/O, digital stereo I/O, and eight-channel ADAT Optical I/O, all via the internal PCI bus on the OCTANE system board. This ASIC is the heart of this audio architecture, serving both as the core of the baseline functionality, and, the PCI/audio interface on each professional digital audio expansion card.

The OCTANE audio system greatly improves the audio capabilities and audio/video synchronization facilities over previous products, while providing 100% audio library compatibility. OCTANE's native capabilities can be augmented by up to three PCI digital audio cards. In addition to professional audio/video synchronization functions, each card can add another set of coaxial digital stereo I/O (AES3) and ADAT Optical 8-channel I/O.

Audio Features

- Standard Analog Inputs
  - Mono electret microphone level input
  - Mono microphone line level input
  - Stereo - 10 dBV line level input

  - Stereo 18-bit analog-to-digital converter
- Standard Analog Outputs
  - Workstation-powered stereo desktop loudspeakers with headphone output
  - Stereo - 10 dBV line level output
  - Stereo 18-bit digital-to-analog converter
- Standard Digital Audio I/O
  - Stereo 24-bit AES3/IEC958 (optical and coaxial)
  - 8-channel, 24-bit ADAT Optical digital interface
- Standard Audio Sample Rates
  - 4KHz - 50KHz, continuously variable
  - Any analog or digital I/O sample rate may be locked to any video or digital audio input
  - Digital-to-analog converter provides jitter attenuation at any sample rate
  - Supports independent sample rates for each audio interface
- Standard Audio Connectors
  - Microphone: 3.5 mm stereo phone jack
  - Speaker/headphones: 3.5 mm stereo phone jack
  - Line In/Line Out: RCA
  - Coaxial Digital (AES-3id): RCA
  - Optical: 12.8 Mb/s EIJA RCZ-6901
- PCI Audio Option Card
  - 8-channel, 24-bit ADAT Optical I/O
  - Stereo 24-bit AES3/IEC958 I/O (optical and BNC coaxial)
  - Video composite sync loop-through. Locks audio sample rates to video
  - Jitter attenuation of digital input clocks
  - Sample-accurate synchronization to other digital media subsystems
  - OCTANE supports up to three option cards per system

Some of the key features of the OCTANE audio system are listed below.

### 3.1.1 Software Compatibility

The hardware and software infrastructure of the OCTANE system represents a significant change and improvement in audio capabilities over previous generations. The Application Programming Interface (API) to the audio hardware, called the Audio Library (AL), has been expanded to encompass new types of audio interfaces, facilitate enhanced programmability of previously-used interfaces, and offers major improvements in synchronization capability. Even with these new advancements, the OCTANE audio system retains source and object code backward compatibility with previous versions of the audio library.

### 3.1.2 Synchronization

Applications such as film and video post-production demand a high level of synchronization capabilities from the hardware. The entire OCTANE audio architecture is designed as a general solution to the problem of guaranteeing precise and long-term synchronization between independent streams of digital media.

The mechanism used for synchronizing independent digital media streams requires two major components:

- maintaining a specific relationship between the media sample rates
- knowledge of each sample's location on a shared time-line

Many system components are used to support this mechanism.

The sample rate for each audio input or output interface may be independently derived from a variety of sources of master timing including internal crystal-based clocks, coaxial and optical serial digital audio inputs, and video reference timing. Interfaces other than the serial digital audio inputs, which are self-clocking, can use a sample rate that is programmed precisely as the product of a programmable rational fraction and the master clock source rate. Many specific ratios are required to service the multitude of relationships between clock rates, hence the reason for incorporating a generalized rational fraction mechanism into the hardware.

A synchronization 'backbone' is built into the OCTANE audio system. This 'backbone' distributes a station reference in the form of a video reference timing signal to all subsystems. These subsystems can utilize the timing signal to derive related media sample rates. In addition, a clock signal which defines a time line agreed upon by all media subsystems is distributed by means of this 'backbone'. In the OCTANE audio system, the baseline audio subsystem generates this clock signal. The source of the backbone video reference timing signal is selected by software from several candidates. Each of the digital media audio and video option cards is capable of generating this signal, including PCI-based audio option cards.

The digital media APIs, including the AL, support understanding of the currency of digital media including:

- UST - Unadjusted System Time (the digital media timeline)
- MSC - Media Sample Count (the per-interface sample count)

Each instantiation of the audio subsystem hardware maintains a flow of status information to the computing core which indicates precise relationships between MSC and UST values at the audio I/O connectors. This knowledge is vital to the computations which are needed to relate the independent digital media streams to the same timeline.

### 3.1.3 Scalability

The OCTANE audio architectural model is used throughout most of the Silicon Graphics product line and allows developers and users maximum flexibility in both programming and hardware configuration. Silicon Graphics plans to support the same PCI audio option card in all current workstation platforms, This includes the O2, OCTANE, Onyx2, Origin2000, and Origin200 workstations. The Onyx2 retains the same baseline audio core architecture as well.

This represents an unprecedented level of scalability of audio architecture across the product line. The hardware implementation of the synchronization backbone is present in all products except O2.

### 3.1.4 Architectural Overview

Figure 3.1 shows a high-level overview of the OCTANE audio system. The blocks in this diagram are explained briefly in the following sections. Note that the diagram is split into data flow (on the left-hand side) and control flow (on the right-hand side).

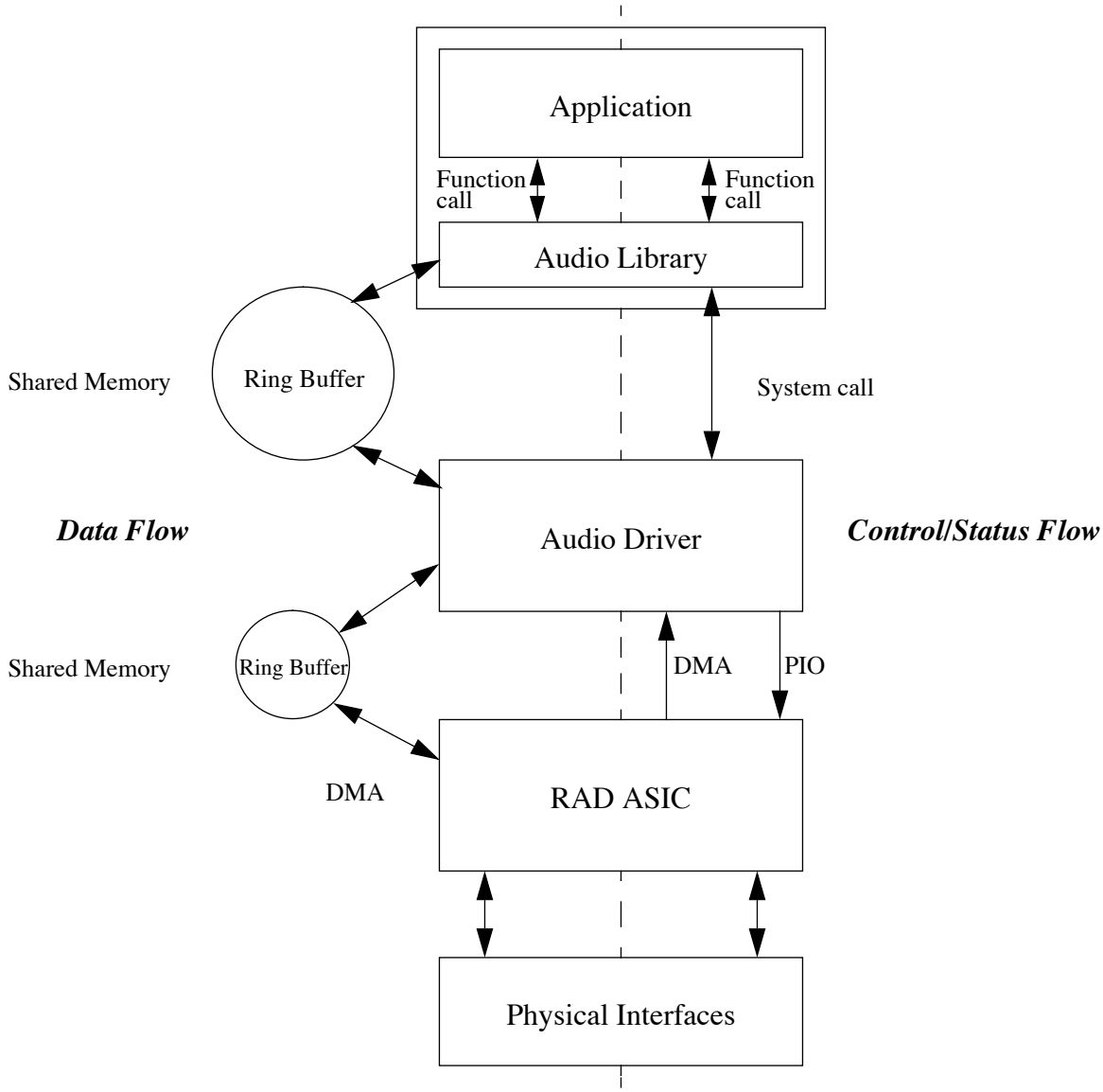


Figure 3.1 Audio System Flow Diagram

#### 3.1.4.1 Audio Library Applications

An audio application is a real-time user-level program running on the CPU. These programs include *Soundtrack*, *Apanel*, *CDman,* and *Midisynth*. These programs interface to the audio system through the Audio Library (AL), which in turn calls the device driver. There are different mechanisms for passing control and data information.

For device control information, the application calls the audio library, which typically executes a system call to pass the request to the device driver.

For data, the application and the device driver share a ring-buffer in main memory. The ring-buffer allows the application to read and write audio data directly without the overhead of a system call. The AL also converts between the application's data format and its own internal format.

#### 3.1.4.2 Device Driver

The device driver is responsible for managing the audio devices on behalf of the applications. The device driver performs the following functions:

- Fan-in of audio data and control from multiple applications (mixing).
- Fan-out of audio data and control to multiple applications.
- Translating generic control information on the application side to and from device-specific control information.
- Managing access to shared resources.

The device driver is divided into two halves which execute concurrently. The top half of the driver is called through the system-call interface from the application. The bottom half of the driver is an interrupt service routine which performs time-critical operations every millisecond. The millisecond time period is derived from the frequency of the fast timer interrupt.

Data flow in the device driver is managed primarily through the interrupt service routine. Each millisecond, the driver receives an interrupt and moves a small amount of data on behalf of each application to or from each device to which the application is connected. The driver also gathers up-to-date status information from each device and makes this information available to the top half of the driver.

Control flow in the device driver is typically achieved through the system-call interface. An application makes a request for a parameter change on a particular device, and the top half either immediately performs the appropriate action, or registers a request for the bottom half to perform the action upon the next interrupt. If an application requests device status, the top half can usually return it immediately since the interrupt routine keeps the most recent status available.

#### 3.1.4.3 RAD ASIC

The RAD ASIC is the main control element of the baseline audio system. The RAD ASIC processes all incoming data from the analog, digital, and ADAT Optical interfaces, and generates all outgoing data. ADAT Optical transmit and receive signals, as well as the digital

stereo output signal are connected directly to the RAD ASIC. The digital stereo input and both analog I/O signals interface to the RAD ASIC through discrete signal translation devices as shown in the audio block diagram.

#### 3.1.4.4 Ring Buffers

The ring-buffers are located in shared memory. One ring-buffer is used as temporary storage for data being passed from the AL to the device driver. The other is used for DMA data transfers between the audio driver and the RAD ASIC.

### 3.1.5 Audio Configurations

The OCTANE system incorporates a baseline audio system along with a PCI bus interface for connection to add-in audio cards. The baseline audio system is shown in Figure 3.2.

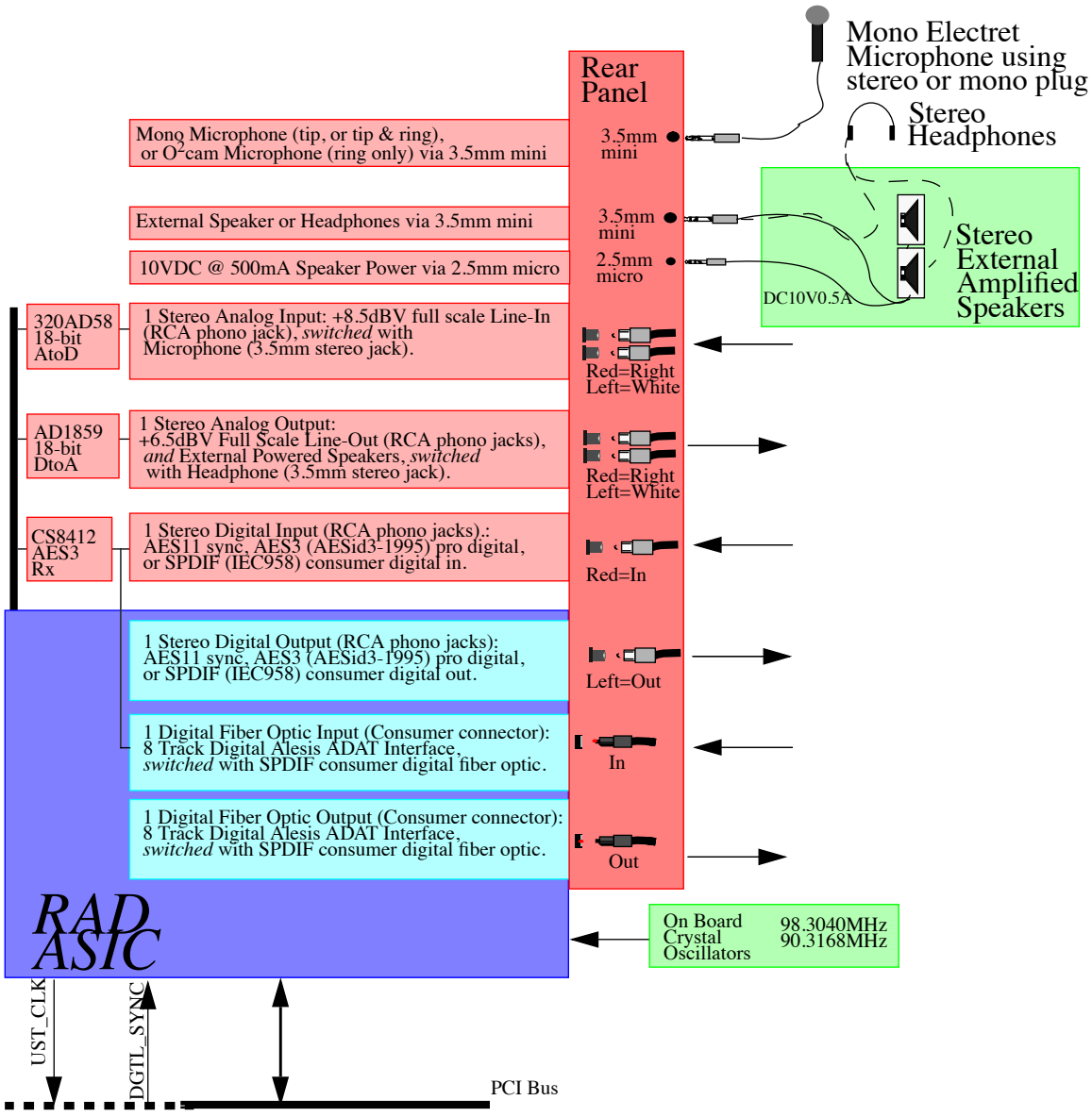


Figure 3.2 Baseline Audio System Block Diagram

#### 3.1.5.1 Baseline Audio System

The baseline audio system consists of the RAD ASIC and numerous stand-alone signal translation devices. These devices provide analog stereo, coaxial digital stereo, and ADAT Optical 8-channel interfaces which are available at the rear panel of the OCTANE system.

Stereo analog line level connections are made directly to the RCA jacks on the rear panel. Signal levels are compatible with consumer equipment such as tape decks, tuners, and amplifiers, as well as professional audio gear.

**Analog Interface**

The analog interface includes a mono microphone input jack which automatically selects between electret microphone level and line-level inputs on its input plug, a speaker/headphone output jack, two line-level stereo analog RCA input jacks, and two line-level stereo analog RCA output jacks.

Signals from the stereo analog RCA input jacks are multiplexed with the microphone input signal. The multiplexer is controlled via the RAD ASIC. The output of the multiplexer passes through volume control circuitry before reaching the inputs of the 18-bit analog-to-digital converter. The resulting digital signals are then processed by the RAD ASIC. This process is shown in Figure 3.3

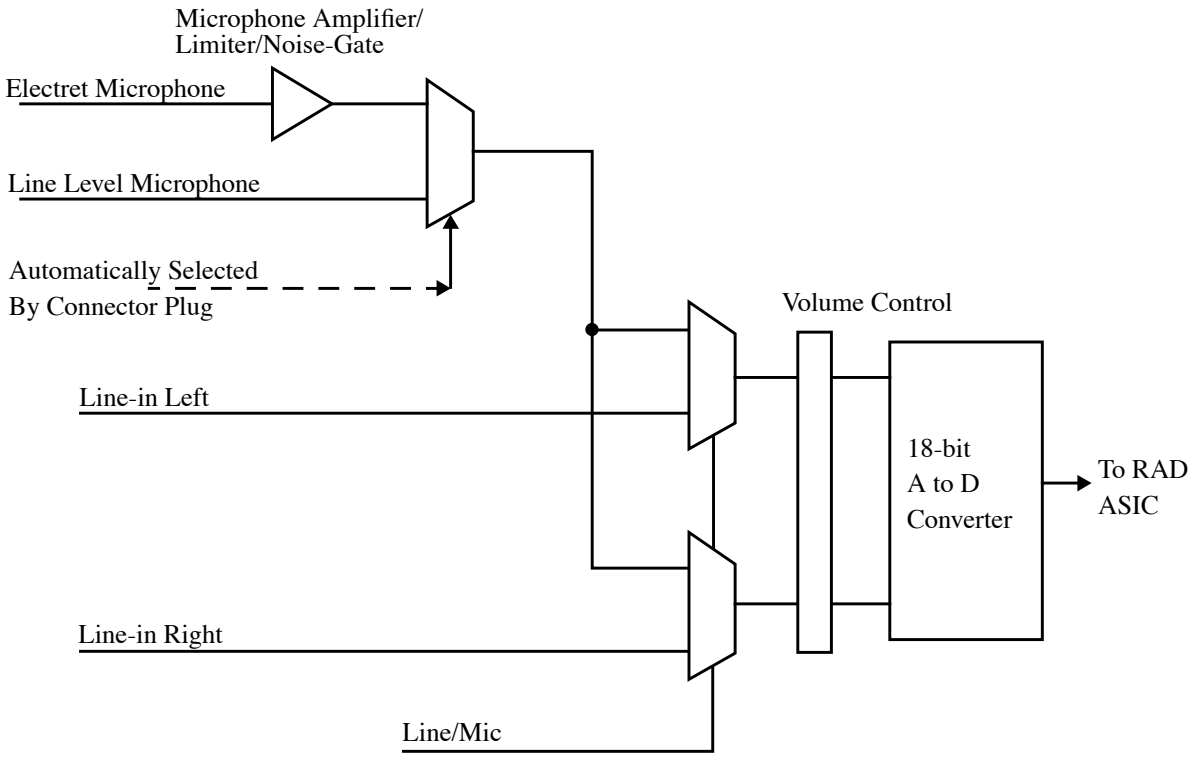


Figure 3.3 Baseline Audio Analog Inputs

The RAD ASIC drives a digital representation of the analog output signal to an 18-bit digital-to-analog converter (DAC) which includes a jitter-attenuating phase-locked loop (PLL) circuit. This PLL circuit significantly improves the analog performance of the converter when the input clock contains high jitter. The analog signal formed by the DAC subsequently drives the line-level stereo analog RCA output jacks. The analog output interface also includes volume control for the 3.5mm stereo speakers/headphone jack, as well as a dedicated 2.5 mm power

jack (10 V 500 mA) that provides power for the desktop speakers. Figure 3.4 shows a block diagram of the analog output interface.

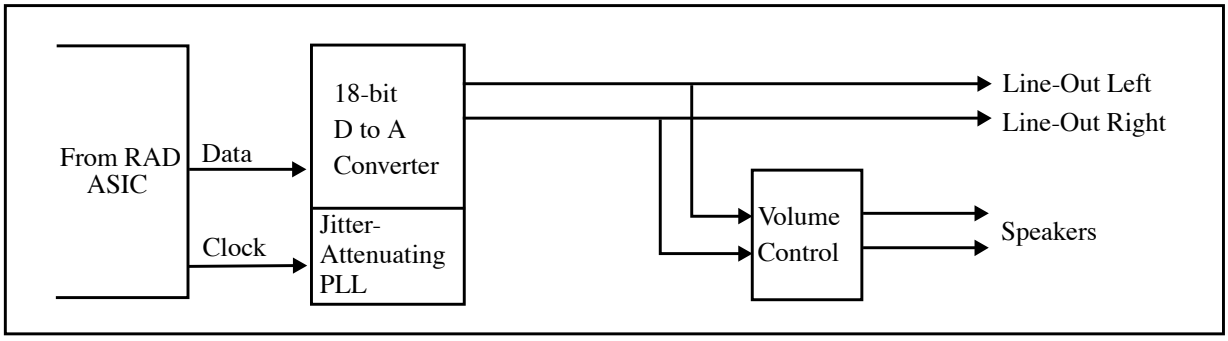


Figure 3.4 Baseline Audio Analog Outputs

**Co-axial stereo digital audio**

RCA jacks on the rear panel support a variety of uses for serial digital audio I/O interfacing. These include a stereo digital data connection to consumer audio products such as DAT (digital audio tape) decks and CD players. This interface is compatible with professional digital audio products as well, conforming to the coding specifications of AES3 and the signal specifications of AES-3id. AES3 supports two-channel (stereo) point-to-point connections using professional sampling rates and a precision of up to 24 bits. AES-3id supports extremely long cable runs using 75-ohm coaxial cable.

In addition to being a data source for the workstation, this input can be used as a timing source for other interfaces in the audio subsystem. For example, the user can choose to lock the sampling clocks of the stereo analog line level output to this input to insure that the streams of audio data through these interfaces move at exactly the same rate.

All of the logic for the stereo serial digital output interface is contained within the RAD ASIC. The stereo serial digital receiver section is implemented with the crystal semiconductor CS8412 device. The RAD ASIC serves as the interface between the CS8412 and the rest of the OCTANE system.

**ADAT Optical Digital Audio I/O**

Each of the digital optical input and output connectors on the rear panel support an 8-channel 24-bit format, the Alesis ADAT Optical interface standard. Originally developed as a proprietary interface for interconnecting Alesis (8-channel, 16-bit) ADAT tape decks, this interface is now widespread across product lines and manufacturers in the professional audio industry.

The same optical interconnection hardware also supports a stereo interface format. The 2-channel (stereo) connection is fundamentally the same signal as described above in the section

on coaxial digital audio I/O. All aspects of the actual signal waveform are the same as for the coaxial digital audio; the only difference is that this signal is carried on multimode plastic fiber material instead of copper wire. The fiber-optic stereo connection is compatible with consumer products such as DAT decks and CD players.

The fiber-optic input, whether receiving ADAT Optical data or the stereo format, can also be used as a timing source for other interfaces (as described above in the coaxial digital audio section).

ADAT Optical receiver and transmitter interface logic is all internal to the RAD ASIC. Optical stereo serial digital audio is received by routing the electrical version of the optical signal to the input of the CS8412; it is then treated exactly as the coaxial digital audio input. The stereo serial digital audio output from the RAD ASIC is multiplexed with the ADAT Optical output signal prior to the optical output transmitter, providing users a choice between ADAT Optical and consumer modes for the optical fiber output.

#### 3.1.5.2 Additional PCI-based Audio

In addition to the powerful baseline audio capabilities of the OCTANE system, up to three PCI Audio Option cards may be integrated via the optional PCI Card cage. Each of these cards adds both another coaxial digital audio and another set of ADAT Optical digital audio connections as well as a video reference timing loop-through. Designed for professional use, the PCI audio option card provides industry-standard BNC jacks for the video and AES connections. Each PCI audio card may derive professional-quality audio timing from the video reference and can propagate it externally as an AES11 audio timing reference signal. The card can also drive the internal video timing reference bus for use by other option cards and the baseline audio system, and provides two built-in Grade2 AES11 reference clocks. An OCTANE system configured with three PCI audio option cards integrates a total of 32 channels of 24-bit ADAT Optical I/O, eight channels of 24-bit AES I/O, and two channels of analog line level I/O.

### 3.1.6 The RAD ASIC

The RAD ASIC is the heart of the OCTANE baseline audio system. The RAD ASIC can be divided into three general areas:

- Data flow
- Control and status management
- Sample-rate generation

This section gives an overview of these functions.

**Data Flow** - The data-flow portion of the RAD ASIC functions as a smart DMA engine, interfacing from the PCI bus on one side to several specific audio interfaces on the other. These interfaces include:

- Analog Devices AD1859 stereo 18-bit digital-to-analog converter
- Texas Instruments 320AD58 stereo 18-bit analog -to-digital converter
- Alesis ADAT 8-channel optical digital input
- Alesis ADAT 8-channel optical digital output

- Crystal Semiconductor CS8412 AES3 stereo digital audio receiver
- AES3 stereo digital audio output

For the AES3 and ADAT Optical inputs and outputs, the RAD ASIC actually maintains two data streams: one stream for the audio data, and one lower bandwidth stream for the non-audio, or "subcode" information. Support is provided for correlating the position of the subcode precisely to the audio data stream.

**Control and Status Management** - The control/status-flow portion of the RAD ASIC performs the following tasks:

- Obtains precise UST/MSC time stamps for each sample frame input and output.
- Controls its internal sample-rate generators.
- Controls and obtains status of all the above-mentioned physical interfaces, including devices external to the chip, such as digitally-controlled analog audio gain and path select.

The RAD ASIC adopts a new approach for returning status information to the host. Because audio is a low-latency real-time function, up-to-date status on all of the audio streams is frequently required. RAD returns this status information via the on-chip DMA engine, which is an improvement over the Programmable I/O (PIO) used in previous generations for transferring status information.

**Sample-rate Generation** - The RAD ASIC contains a general solution to the problem of audio sample-rate generation for multiple selectively-synchronized audio interfaces. Each audio interface that receives a sampling clock from the RAD ASIC can independently select a frequency that has a precise (rational) fractional relationship to a "master" timing source. The precision of these fractional relationships guarantees an absence of long-term drift between audio streams and the master timing sources. Master timing sources include coaxial and optical digital audio inputs, and on-board crystal-based oscillators.

Sample rates may also be selected with reference to video timing rates. For example, it is straightforward to specify that the digital-to-analog converter interface should receive a sampling rate of 44.1 KHz (the CD sample rate) with respect to the OCTANE's internal video reference timing bus, whether the video is in NTSC or PAL format.

In addition to these generalized frequency synthesis capabilities, the RAD ASIC provides the structure to utilize additional circuitry to provide jitter attenuation for synthesized sampling clocks. This circuitry is implemented on a PCI digital audio expansion card.

Interfaces that receive synthesized sampling clocks from the RAD ASIC include the A/D converter, D/A converter, the AES3 transmitter, and the ADAT Optical interface transmitter.

### 3.1.7 Standard Audio Peripherals

#### 3.1.7.1 Microphone

The standard OCTANE audio system includes a high-quality electret condenser monaural microphone. The microphone has a directional response, a wide frequency response, and a large dynamic range.

The microphone input circuit provides DC power for active circuitry in microphones that require it, while retaining compatibility with other types of microphones. Powered microphones, such as the one supplied with the OCTANE system, use this DC power to drive a large low-impedance signal back to the audio circuitry, avoiding the problems associated with low-level microphone signals and electrically noisy computer environments.

The microphone input circuit also accepts monaural line level microphones via the same 3.5mm connector; in this case the input signal should be provided on the “ring” of the tip-ring-sleeve assembly. The DC power feature, noise gate, limiter, and hardware 30 dB gain stage are automatically disabled when a plug with the tip either grounded or “no connect” is used.

#### 3.1.7.2 Desktop Loudspeakers

The standard OCTANE audio system includes a pair of desktop loudspeakers. The user can experience a stereo sound field by placing them adjacent to their desktop graphics monitor.

The speakers receive power through a specialized 2.5mm phone jack, and obtain their audio signals via the standard 3.5mm stereo headphone jack on the OCTANE’s rear panel. The right loudspeaker provides some other conveniences; a headphone jack, loudspeaker power switch, and a low-frequency boost control.

Inserting a headphone plug into the headphone jack on the loudspeaker disables the loudspeakers. The power switch also serves as a mute control; no sound propagates through the loudspeakers when the power switch is in the “off” position. Volume control for loudspeakers and headphones is provided in the workstation. Typically, users will use the *Apanel* application to control the volume. The headphone jack at the rear of the workstation is also directly compatible with headphones.

# *Section 4 Graphics Architecture*

The OCTANE system provides state-of-the-art graphics capability which supports both 2D and 3D imaging. The OCTANE graphics subsystem is similar to that of the previous generation Impact graphics architecture, with the following upgrades:

- higher performance bus interface ASIC (HQ4)
- updated alpha and intensity texture formats in the Raster engine (RE4)
- 4MB of Texture RAM standard
- supports an expanded number of screen resolutions

The OCTANE graphics subsystem is available in four configurations which use variations of the same components. The following is a list of features. Note that not all features are available on all graphics configurations.

- 36-bit color buffers (12-bits per component RGB)
- 32-bit color buffers (8-bits per component RGBA)
- 12-bit color index buffers
- 24-bit depth buffer
- 8-bit stencil buffer
- 8-bit overlay
- up to 1600x1200 screen resolution*
- HDTV resolution support*
- quad-buffered stereo display in a window**
- up to 119M pixels per second trilinear mipmapped texture performance*
- highest quality anti-aliased lines at interactive speeds
- over 1.1 million smooth shaded, textured, Z-buffered, fogged triangles per second*
- hardware support for up to 7x7 general and separable convolutions
- 60Mtexel per second texture download rate
- hardware accelerated off-screen buffers (pbuffers)
- hardware support for curve and surface evaluation
- enhanced alpha and intensity texture support

*These features are only supported on the OCTANE/MXI graphics configuration.
**Standard on MXI graphics, optional on SI graphics.

## 4.1 Graphics Configurations

This section explains each graphics configuration. The four graphics configurations are:

- SI - Solid Impact
- SI with Texture Option

- SSI - Super Solid Impact
- MXI - Maximum Impact

Table 4.1 shows a listing of the major components available in the various graphics configurations. The names in parentheses relate to the block diagrams in Figure 4.1 through Figure 4.4.

Table 4.1 OCTANE Graphics Configurations

| Component | Graphics Subsystem | | | |
|---|---|---|---|---|
| | SI | SI with Texture | SSI | MXI |
| Geometry Engine (GE11) | 1 | 1 | 2 | 2 |
| Raster Engine (RE4) | 1 | 1 | 2 | 2 |
| Texture Engine (TE1) | -- | 1 | -- | 2 |
| Texture memory (TRAM) | -- | 4MB | -- | 8MB |
| Pixel Engine (PP1) | 2 | 2 | 4 | 4 |
| Color Mapper (CMAP) | 2 | 2 | 2 | 2 |
| Pixel Memory (RDRAM) | 12MB | 12MB | 24MB | 24MB |

### 4.1.1 Solid Impact (SI)

The *Solid Impact* (SI) is the baseline graphics subsystem. The SI graphics subsystem contains one Geometry Engine (GE11), one Raster Engine (RE4), two Pixel Engines (PP1), and 12MB of pixel memory. Texture mapping is not supported in the SI graphics configuration. Figure 4.1 shows a block diagram of the SI graphics subsystem. Each of the components in Figure 4.1 are defined in Section 4.2.

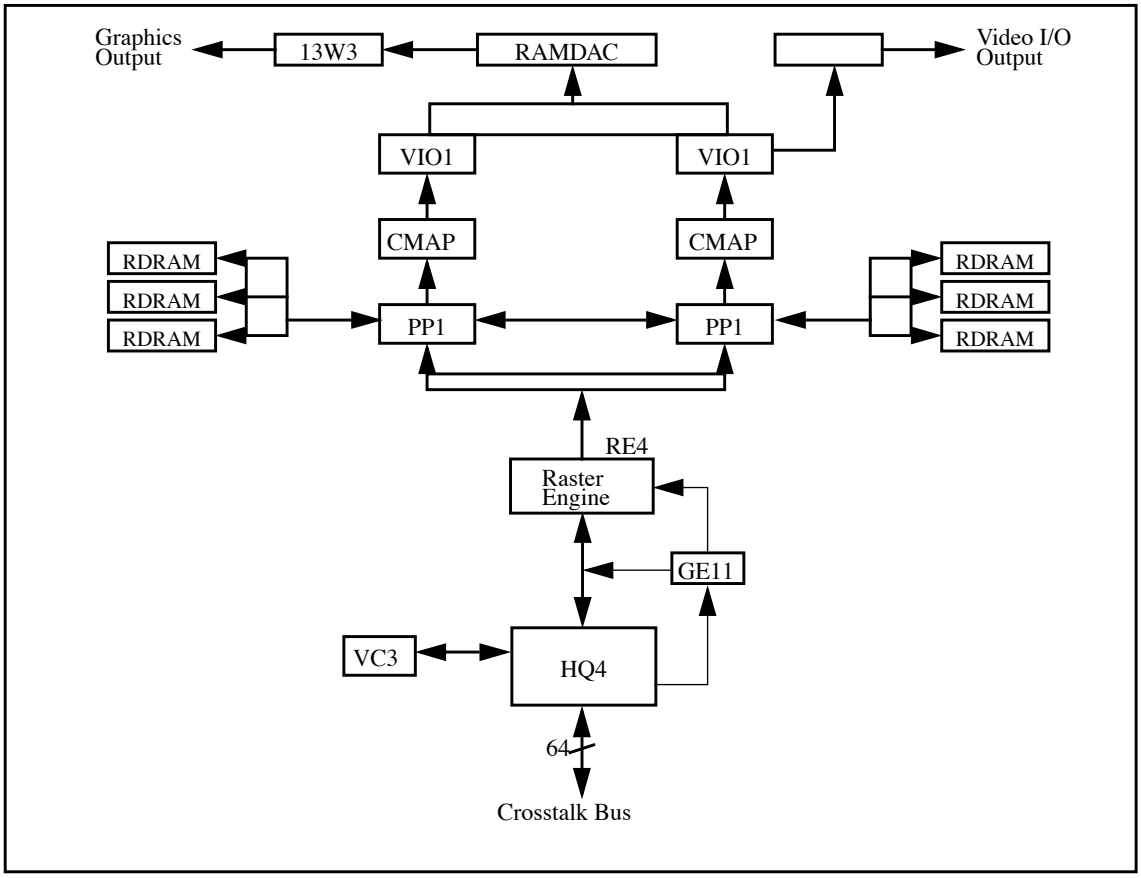


Figure 4.1 SI Graphics

### 4.1.2 Solid Impact with Texture Option

The *Solid Impact with Texture Option* configuration is identical to the SI baseline graphics subsystem shown in Figure 4.1, with the addition of texture. The texture option is available on a daughtercard which connects to the SI graphics board. The SI with Texture Option graphics subsystem contains one Geometry Engine (GE11), one Raster Engine (RE4), one Texture Engine (TE), 4MB of Texture RAM (TRAM), two Pixel Engines (PP1), and 12MB of pixel memory. Figure 4.2 shows a block diagram of the SI with Texture Option graphics subsystem. Each of the components in Figure 4.2 are defined in Section 4.2.

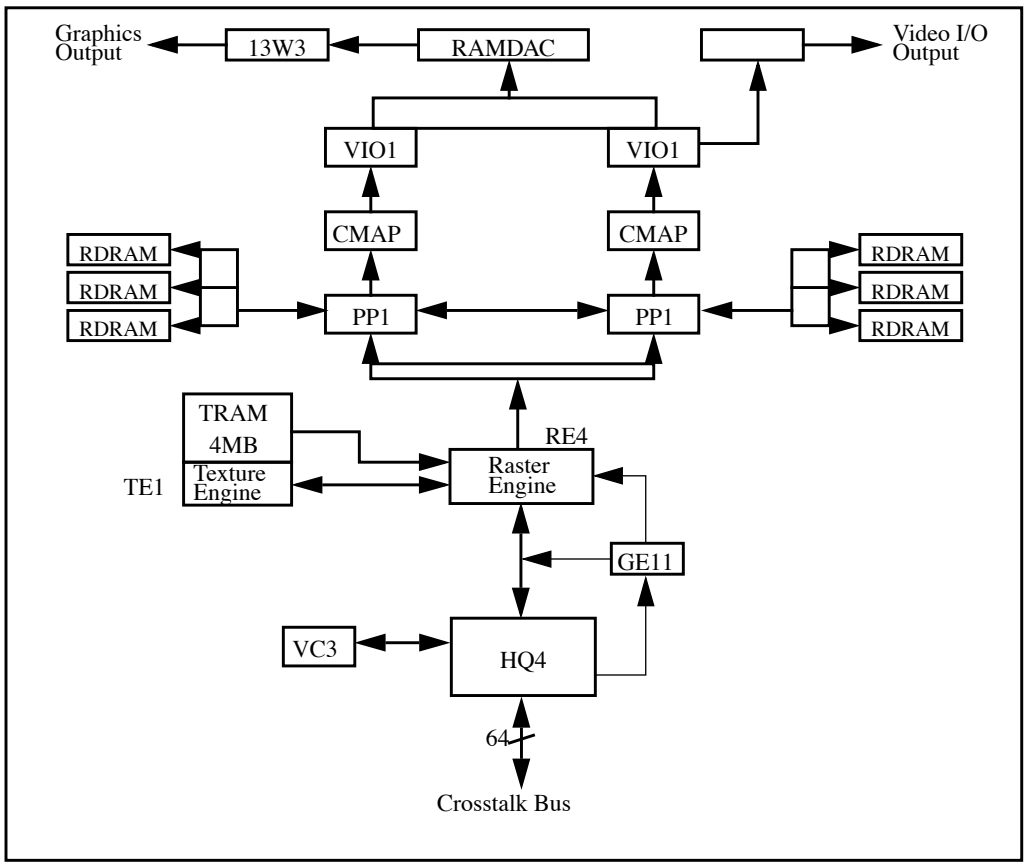


Figure 4.2 SI Graphics with Texture Option

### 4.1.3 Super Solid Impact (SSI)

The *Super Solid Impact* (SI) graphics subsystem incorporates multiple Geometry and Raster Engines, and doubles the amount of pixel memory. The SSI graphics subsystem contains two Geometry Engines (GE11), two Raster Engines (RE4), four Pixel Engines (PP1), and 24MB of pixel memory. Texture mapping is not supported in the SSI graphics configuration. Figure 4.3 shows a block diagram of the SSI graphics subsystem. Each of the components in Figure 4.3 are defined in Section 4.2.

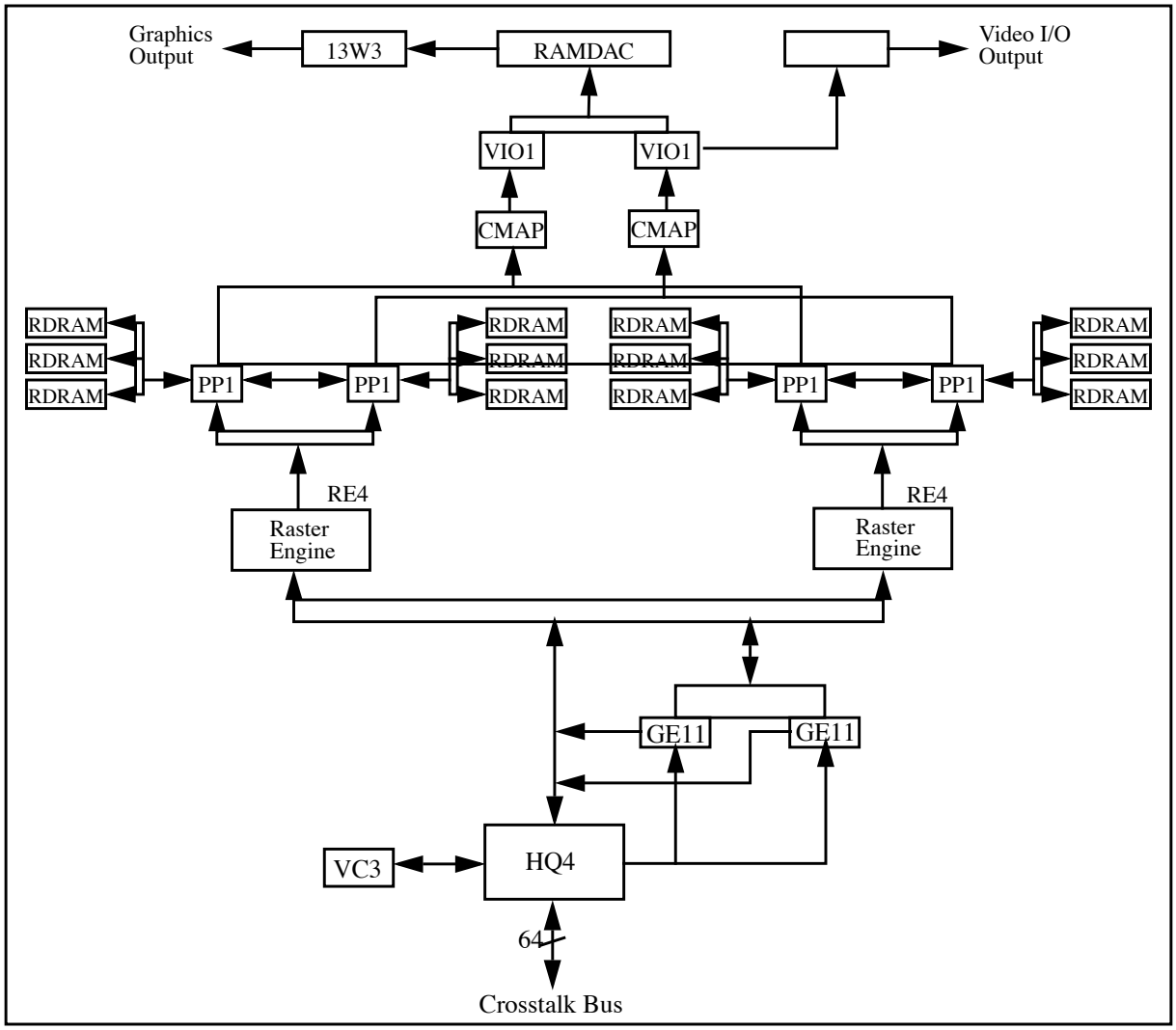


Figure 4.3 SSI Graphics

### 4.1.4 Maximum Impact Option (MXI)

The *Maximum Impact (MXI)* configuration is identical to the SSI graphics subsystem shown in Figure 4.3, with the addition of texture. The texture option is available on a daughtercard which connects to the graphics board. The MXI graphics subsystem contains two Geometry Engines (GE11), two Raster Engines (RE4), two Texture Engines (TE), 8MB of Texture RAM (TRAM), four Pixel Engines (PP1), and 24MB of pixel memory. Figure 4.4 shows a block diagram of the SI with Texture Option graphics subsystem. Each of the components in Figure 4.4 are defined on Section 4.2.

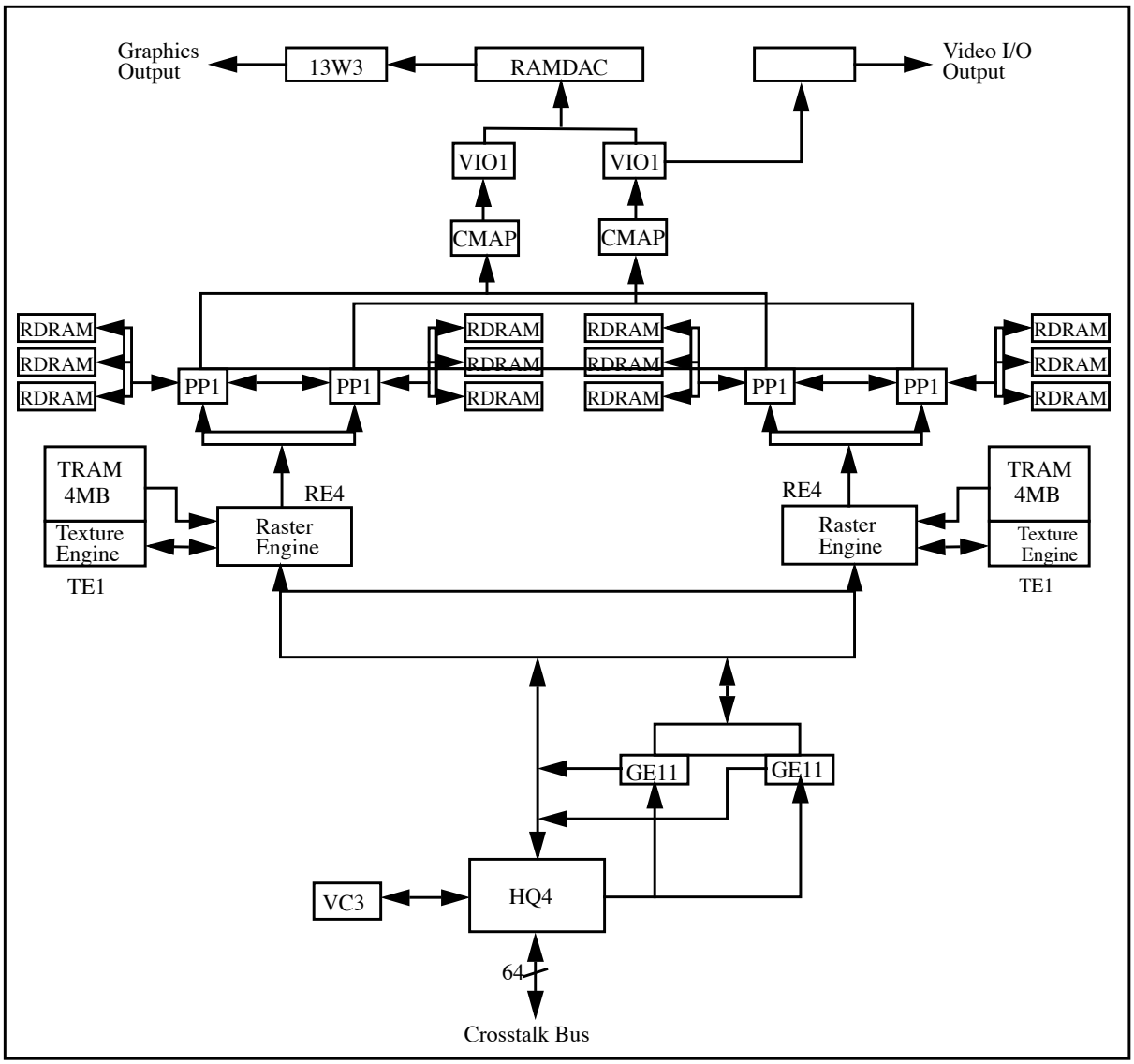


Figure 4.4 MXI Graphics

### 4.2 Graphics Subsystem Components

This section defines each of the ASICs shown in Figure 4.1 through Figure 4.4.

#### 4.2.1 HQ4 - Bus Interface ASIC

The HQ4 ASIC provides the interface between the graphics board and the Crossbow ASIC via the 400MHz Crosstalk bus interface. The HQ4 is responsible for downloading all OpenGL®

state, geometry information, and pixel data and then routing them to the appropriate components for processing.

On those systems with more than one Geometry Engine, the HQ4 performs load balancing based on the filling of the GE11 command FIFOs. The HQ4 is responsible for coordinating context switches and handling DMA in and out of display list and texture information. The HQ4 ASIC supports conversion of all OpenGL® pixel types into the OCTANE hardware's native storage formats.

The HQ4 supports the following types of high-speed transfers:

- straight through, host-to-raster-engine pixel reads and writes
- host to geometry engine and raster engine operators and format conversions
- raster engine to geometry engine pixel operations on screen-to-screen copies
- raster engine or geometry engine to host transfers for pixel read reformatting

The HQ4 also acts as an interface for the GE11(s). By using an internal RAM-based microcode sequencer, the HQ4 can:

- parse the OpenGL instruction stream into primitives for distribution to the GE11(s)
- track OpenGL attributes and update the GE11(s) as needed
- normalize 8- or 12-bit color values
- control REbus ownership and arbitration
- reformat PCI data into raster engine register formats

### 4.2.2 GE11 - Geometry Engine ASIC

The GE11 provides the OCTANE system with over 480 MFLOPS of computational geometry processing power. The GE11 handles matrix manipulations, coordinate transformations, lighting, clipping, culling and other operations required for converting from 3D to 2D as well as image processing operations such as convolutions, color look-ups and histograms. Up to two GE11s are available depending on the graphics configuration.

The GE11 design is a compromise between the functionality of a general purpose CPU and the performance of a hard-wired DSP. Each GE11 contains a command FIFO, address and data register files, and multiple internal first-in-first-out (FIFO) buffers. Since most of the GE11 operations are microcoded and may require external storage, each GE11 has access to pipelined synchronous static random access memory (SSRAMs) which contain data and microcode.

Each GE11 contains three SIMD floating point and integer cores which offer a dual threaded interface to the microcode logic. If multiple GE11 devices are present in a system, they run in MIMD mode, thereby avoiding many of the performance degradations of SIMD machines when they are forced to break out of SIMD.

### 4.2.3 RE4 - Raster Engine

The SSI and MXI graphics configurations each contain two raster engine (RE4) ASICs. Each raster engine works in combination with two pixel processor (PP1) ASICs, and 24MB of pixel

memory to provide a high rasterization and scan out of the frame buffer. The second raster engine handles alternate spans in the frame buffer, effectively doubling the rasterization power.

The GE11 feeds geometry, color, and texture information for triangles, blocks, lines and points to the RE4 ASIC. The RE4 shares some of this information with the TE, enabling it to independently work on textures. The RE4 breaks the primitives that it receives into spans in the XZ plane and works through these spans in the -Y direction. For each pixel in the frame buffer that it is responsible for, the RE4 calculates the X and Y values with 8-bits of subpixel precision and then iterates across the span, generating R,G,B,A and Z values for each pixel. The RE4 iterates R, G, B and A values in 12-bits and Z in 24-bits of precision. Computation of pixel primitives and their associated parameters are passed on to the rendering subsystem.

The RE4 design is capable of generating one span per clock and sending it down to the iteration logic. The iteration logic offers high performance buffer clears, pixel reads and writes, and area fills. A line fill is slightly slower than polygon fill.

In most cases the RE4 performs all fog and texture blending at no additional performance overhead. However, a marked performance degradation occurs when using 12-bit per component texture images, as there is a larger number of 8-bit internal blending units than 12-bit blending units. Moreover, fogging requires use of the same blenders, therefore concurrent texturing and fog, especially with 12-bit components, resulting in additional loss of performance.

The RE4 also supports three 256-entry, 8-bit texture look-up tables for post-interpolation mapping of luminance or RGB textures. In addition, the OCTANE system offers enhanced support for alpha and intensity texture internal formats in the RE4 ASIC. The alpha support controls the amount of transparency in the image and allows the user to blend pixel values in the frame buffer. The result is the enhanced ability to see through objects on the screen. Alpha allows for single-component texturing and the ability to overlay texture onto images that have an irregular shape. The enhanced intensity texture formats allow a single-component texture to affect all four components of the resulting pixel; R, G, B, and alpha. By contrast, the luminance function affects only the R, G, and B components. However, the texture look-up tables are shared with the fog look-up table and therefore should not be used simultaneously.

### 4.2.4 TE1 - Texture Engine

The Texture Engine (TE1) performs the same type of span iteration that the raster engine does, except with spans of texture coordinates. The separation of the two systems prevents one from blocking the other in iterating its set of spans. One texture engine is used with each raster engine.

The TE1 and RE4 ASICs work in conjunction with one another to provide the texture function. The RE4 receives the texture samples from the TRAMs. The RE4 then performs all texture environment blending, fog blending, and alpha blending operations. Figure 4.5 shows a simple diagram of the texture data flow during a texture mapping operation.

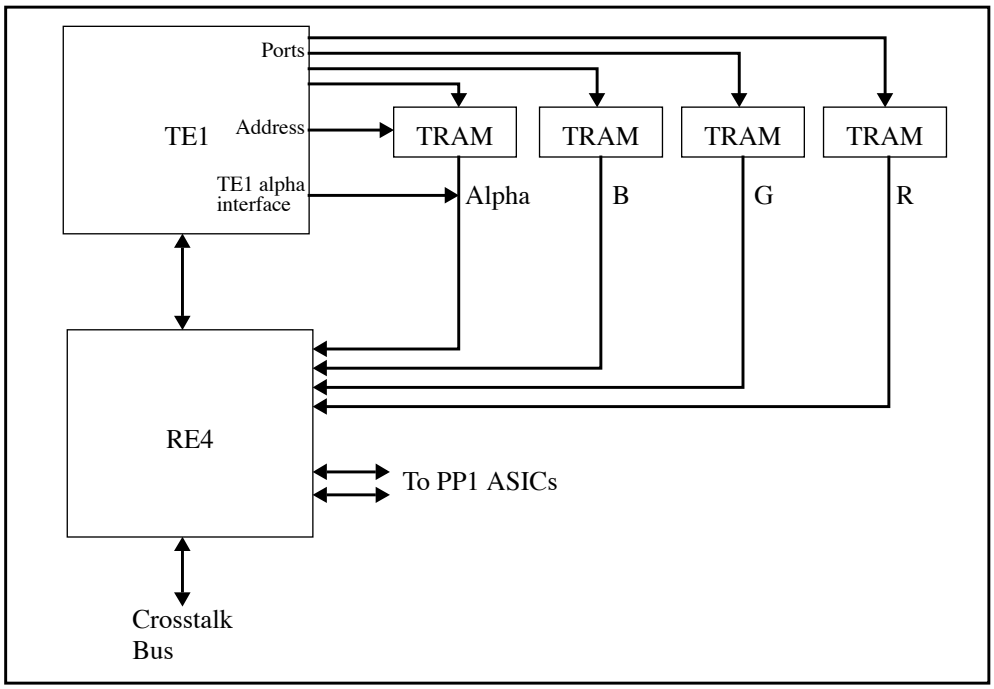


Figure 4.5 Texture Mapping Data Flow

Each texture engine uses 4MB of texture RAM (TRAM) for fast texture mapping. The texture engine interpolates texture coordinates, performs the perspective division, calculates texture level-of-detail and sends the data over a high speed bus to the TRAM. The TRAM pulls out the appropriate texels, filters them and then returns up to two filtered texels per clock to the raster engine.

A texel, or texture element, refers to one location in the texture RAM which contains a small portion of the texture map being used. The OCTANE system supports linear, bilinear and trilinear interpolation. Bi-linear interpolation refers to having four texels per pixel, whereas trilinear interpolation refers to having eight texels per pixel. Tri-linear interpolation offers the highest detail level during texture mapping. Refer to the TRAM description below for more information.

### 4.2.5 TRAM - Texture RAM

The TRAM is the first chip to implement large quantities of texture memory with a texture cache and interpolation processor. One TRAM ASIC is standard with each texture engine. The TRAM ASIC contains 4MB of texture memory and along with the texture engine comprises a daughterboard which connects to the main graphics board. Adding the texture option in the SI graphics configuration requires a single texture daughterboard, whereas adding the texture option in the SSI graphics configuration requires the installation of two texture daughterboards, one for each raster engine.

The TRAM ASIC is what enables the OCTANE system to provide high performance, low cost texture mapping. For example, had the texture memory function been implemented in DRAM, it would have been necessary to provide eighty 4-Mbit parts arranged in a 10-way interleaved configuration in order to achieve the same kind of performance that is available in a single TRAM ASIC.

The TRAM operates off of three basic parameters; the S and T coordinates, and the Level-of-Detail (LOD) value. Every monitor has an X (horizontal) and Y (vertical) coordinate. The on-screen image also has X and Y coordinates. However, the coordinates of the monitor may or may not be the same as the coordinates of the image based on the way the image is oriented on the screen. For this reason, image coordinates are referred to as S and T, where the S-coordinate is actually the X-coordinate of the on-screen image, and the T-coordinate is actually the Y-coordinate of the on-screen image. Figure 4.6 shows the relationship of the X,Y and S,T coordinates.

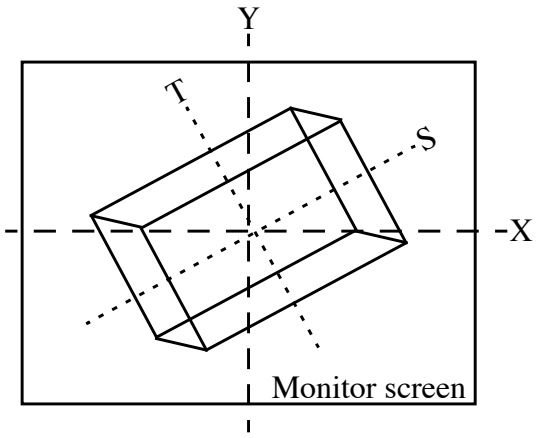


Figure 4.6 Spatial Coordinate Relationships

The LOD value is analogous to the Z-coordinate value in a three dimensional image. The LOD value is based on where the texture map is in relation to the rest of the screen. For example, assume the texture map is the logo on an aircraft wing. If the logo is close-up in the image and requires a relatively large portion of the screen to be mapped, the image will have a correspondingly large LOD value. By contrast, if the airplane wing and logo are in the background of an image and require a relatively small portion of the screen to be mapped, this will be reflected by a smaller LOD value. In general, the LOD value indicates which picture to get texture samples from, and the S and T coordinates indicate where in that picture to get the texture samples from.

Based on the S, T, and LOD values, the TRAM fetches the appropriate texels and performs a linear, bilinear, or trilinear sample before returning a filtered texel. Because of the TRAM's texel management, trilinear mipmap (highest quality) sampling is the fastest mode. Bilinear or point sampling may be significantly slower under minification, depending on the size of the texture. 3D texturing will also result in some performance degradation due to the caching algorithm implemented within the TRAM.

The DRAM array implemented in the TRAM ASIC is banked so as to allow simultaneous sampling and loading of different textures. Texture loads are possible at 60 Mtexels per second. This is currently the fastest texture load performance of any desktop system in existence today. This performance can be critical for those applications which cannot store all the textures they use in 4MB of memory or environments in which there are multiple applications contending for texture memory.

The 4MB TRAM allows use of up to 48-bit texels. There is no difference in sampling speed, although 12-bit per component textures cannot be sampled and loaded at the same time unless they are in luminance format.

Texture residency in the TRAM is determined by the OpenGL layer. Several heuristics are currently used to determine which textures, and which parts of which textures should be stored in the TRAM. Note that since texture memory is shared among applications, this is not an easy problem. Since this is programmable, ISVs for whom texture residency is a critical issue should contact Silicon Graphics to determine what the heuristics are for the current software release. There may also be extensions to OpenGL (they are a part of OpenGL 1.1) that can be used to help prioritize this residency.

### 4.2.6 HRBE - High Resolution Back End Circuitry

The HRBE consists of:

- a VC3 high-resolution timing display generator
- two VIO1 video interface ASICs
- two color map ICs (CMAPs)
- one RAMDAC digital to analog convertor
- one 13W3 video connector

#### VIO1 - VIDEO I/O

The VIO1 mentioned in the previous subsection has three functional connection lines:

- the outputs received from the color map IC
- an output line to the RAMDAC IC
- a bidirectional (input and output) bus that can connect to an optional Video, ICO, or Presenter board

## 4.3 Graphics Data Flow

This section describes the general flow of data through the graphics subsystem. Figure 4.7 shows the general flow and includes all OCTANE graphics configurations. The diagram contains numbers at various points in the data flow. These numbers equate to the numerical sequence below that explains the operations performed at each point.

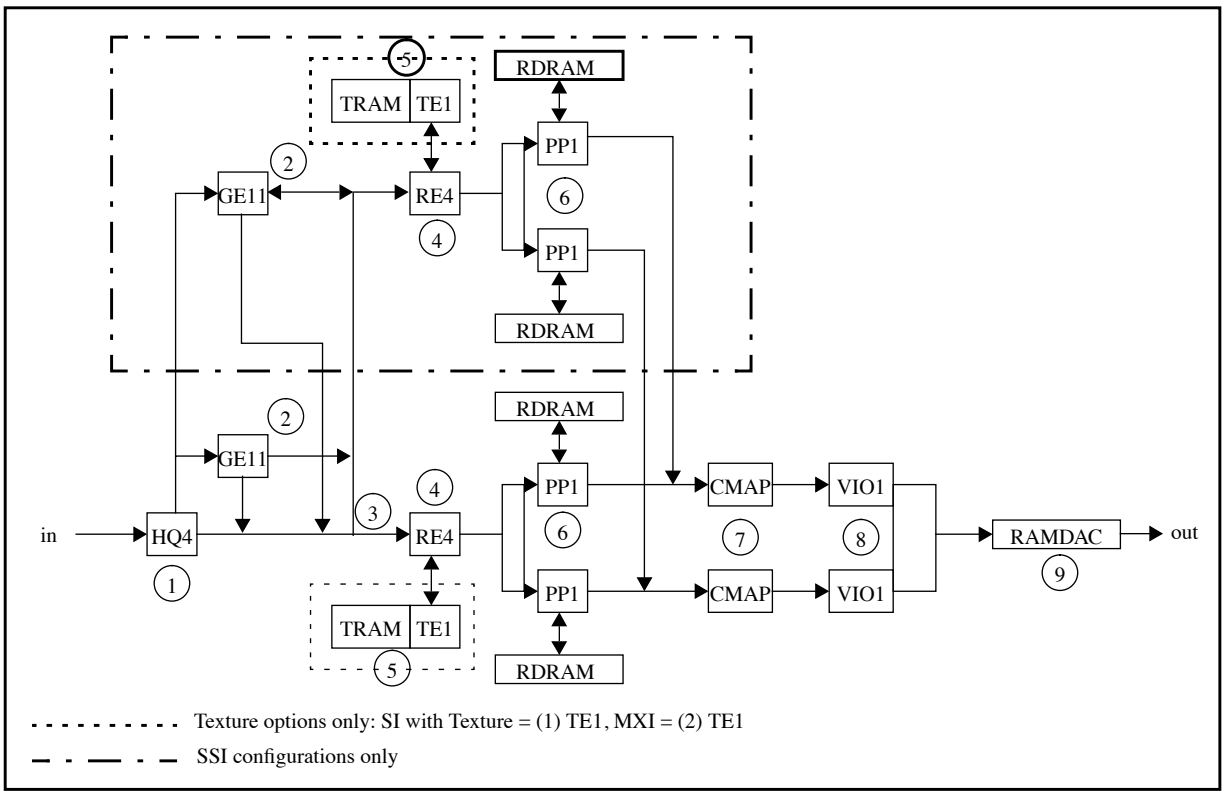


Figure 4.7 Graphics Subsystem Data Flow

1. A graphics cycle originates with the host sending the graphics operation to the HQ4 ASIC. This ASIC contains a FIFO which stores the commands of the operation.
2. The HQ4 first sends these commands to the GE11. The GE11 converts 3D coordinates into 2D screen space and performs matrix manipulations, coordinate transformations, lighting, clipping, culling and other operations.
3. The converted data is sent directly to the appropriate raster engine. In the SI graphics configurations, one raster engine (RE4) is used to processor both odd and even horizontal screen lines. In the SSI graphics configurations, two raster engines are used. One RE4 is used to process even horizontal lines, while the other is used for odd horizontal lines.
4. The RE4 ASIC iterates across each scan line and generates the color of each pixel on a given horizontal line based on the starting and ending colors of that line. When attached to a texture engine (TE1), the RE4 also performs texture blending and fogging operations. Once this information has been calculated, the RE4 outputs the data to the pixel engine (PP1) where it is written into the RDRAM pixel memory.
5. In those graphics configuration which include the texture option, the TE1 ASIC performs the same relative function as the RE4, only for texture. The TE1 interpolates texture coordinates and computes texture level-of-detail, passing the data to the texture RAM (TRAM) for texel look-up and filtering.
6. The PP1 ASIC is a pixel processor which writes back and forth to the pixel memory (RDRAMs). The PP1 performs pixel operations such as alpha test, depth test, stencil operations, blending, dithering, and masking. Each of these processes is explained in Section 4.4, OCTANE Graphics Features. In addition, the PP1 performs Z-buffering operations, performing read-modify-write operations to the RDRAMs. The SI graphics configurations contain two PP1 ASICs and 12MB of

RDRAM memory, whereas the SSI graphics configurations contain four PP1 ASICs and 24MB of RDRAM memory.

7. The PP1 devices output the data to the Color Map (CMAP) ASICs. These ASICs contain a color look-up table of raw pixel values which must be mapped to the color space being used. The CMAP devices also perform gamma correction.
8. Each CMAP device outputs data to its own VIO1 video controller which converts scanned-out video prior to being input to the RAMDAC. The VIO1 device performs video multiplexing for both video and compression.
9. The RAMDAC converts the data to its analog equivalent where it is sent to the monitor for display.

## 4.4 OCTANE Graphics Features

### 4.4.1 MicroPixel Sub-Pixel Positioning

After being projected to the screen by the geometry subsystem, all vertices retain 8-bits of fractional positioning information instead of being coerced into integers. This gives an accurate description of the primitive's position in a floating-point space. Without this feature, primitives would be rendered incorrectly and would jitter as they move, also causing serious problems with the anti-aliasing features described below.

### 4.4.2 Blending

OCTANE graphics supports both source and destination alpha for complete composition capabilities. The pixel data in the frame buffer is replaced with a weighted average of itself and the pixel data being drawn. The user selects the function controlling both the source and destination factors used in the blend.

One common blend operation uses the alpha component of the pixel being drawn as the source factor and one-minus-alpha as the destination factor. The greater the alpha value, the more weight is given to the incoming data in the blend. This method is used to draw anti-aliased lines and to generate transparencies. It can be used any time subpixel coverage is demanded.

OCTANE also supports a number of extended blending modes. One of these sets the blend equation so that each component of the resultant color is the minimum or maximum of the corresponding component of the source and destination color. This is particularly useful in medical volume rendering for calculating the Maximum Intensity Projection (MIP). Another blending equation allows any bit-wise logical operation to be applied to each of the source and destination color components. Two more blend equations allow subtraction instead of addition in blending the source and destination components. The “subtract” equation subtracts the product of the destination factor and destination color from the product of the source factor and source color. The “reverse subtract” does the opposite, subtracting the source product from the destination product. Blend subtraction is useful for finding differences between two images. Finally, a constant color or constant alpha can be chosen as the source or destination factor allowing for efficient fades and blending between two images.

### 4.4.3 Point Anti-Aliasing

To render an anti-aliased point, a 2 x 2 grid of pixels is used to approximate the area covered by a filtered point. The four pixels are given blend weights proportional to the distance from their pixel centers to the actual point location in sub-pixel space.

### 4.4.4 Line Anti-Aliasing

Lines are anti-aliased by drawing a 2-pixel-wide line with higher weights for pixels closer to the line in the minor axis, and lower values toward the outer pixels. This technique effectively approximates the location of a line by a wide line that is filtered in the minor axis. Similar to points, RGB lines are blended into the frame buffer by the weights. For color indexed anti-aliased lines, instead of generating a weight for blending, the hardware substitutes the lower 4-bits of the color index value. The new color then indexes into a ramp in the color look-up tables.

#### 4.4.4.1 Slope Correction

OCTANE graphics automatically adjusts pixel intensity so that a line appears uniform at all angles.

#### 4.4.4.2 End-point Filtering

So far, the weights of pixels that make up anti-aliased lines have been adjusted only in the minor axis. The end points of the lines must also be adjusted in the major axis to avoid popping from one pixel to the next. To correct this, the hardware uses the subpixel information in the major axis to adjust the intensity of the endpoint color. This way the apparent endpoint moves gradually from one pixel to the next.

### 4.4.5 Accumulation Buffer

OCTANE graphics offer a 64-bit software accumulation buffer to combine or accumulate a set of scenes. The OpenGL Graphics Library API also allows for a weighted blend of each of the scenes into the accumulated image. The weight of each scene is defined by the user. These weights can be used with other features of the graphics subsystem such as a projection matrix to define User-Programmed Filter Functions.

#### 4.4.5.1 Progressive Refinement

As each frame is stored into the accumulation buffer, a more accurately sampled image is produced. The user can choose to render fewer frames to support real-time constraints, or to render many frames to obtain a high-quality image.

#### 4.4.5.2 Multi-Pass Spatial Anti-Aliasing

Multi-Pass Spatial Anti-Aliasing is done by rendering the same objects for several frames while moving them spatially. By jittering the subpixel offsets (i.e., projection matrix) and accumulating the scenes together, an anti-aliased image is rendered. Furthermore, the user can choose a desired filter function to define the weights for each pass.

#### 4.4.5.3 Optical Effects

By modifying the projection matrix as images are accumulated, such as viewing the scene from various points across the aperture of a lens, a sense of depth-of-field is created. Objects that are further from the focal plane of the lens are blurred while closer objects are made sharper.

#### 4.4.5.4 Convolutions

An image can be quickly filtered using the accumulation buffer. Since the user has control of the weighted accumulation of each image, and the image can be moved about on screen in multiples of pixel coordinates, the accumulation buffer can be used to convolve the image using many filtering techniques. Convolution is also supported by the GE11 ASIC using a pixel operation for image processing.

#### 4.4.5.5 Orthogonality

The accumulation buffer provides a solution for the problem of spatial aliasing, motion-blur, depth of field, and penumbra. Another feature of the accumulation buffer is that all these techniques can be used together in any combination to render a high-quality image.

### 4.4.6 Lighting Features

The OCTANE architecture supports a wide range of lighting capabilities to enable the realistic rendering of geometric primitives. Lighting effects are computed on a per-vertex basis (Gourard lighting) and are thus supported in the geometry engines.

All OCTANE graphics configurations support all of the following OpenGL Graphics Library API lighting capabilities in hardware.

#### 4.4.6.1 Light Sources

Up to eight light sources may be used simultaneously. The user can specify the color and position of each light source.

#### 4.4.6.2 Surface Properties

The OpenGL Graphics Library API allows the user to configure a number of surface properties to achieve a high degree of realism. Specifically, the user can define the emissivity of a surface and its ambient, diffuse, or specular reflectivity, as well as its transparency coefficients. A shininess coefficient is provided to specify how reflective an object is. The Command Processor and Geometry Engines were specifically designed so that surface properties can be quickly modified on a per-vertex basis. This feature is particularly useful for scientific visualization. For example, an aeronautical engineer can change the diffuse reflectance at every vertex to show the stress contour across an airplane wing.

#### 4.4.6.3 Two-Sided Lighting

The user can specify different surface properties for the front and back sides of geometric primitives to display objects whose inside and outside colors differ. This obviates the need to specify and render two separate primitives.

### 4.4.7 Local Light and Viewer Positioning

Traditionally, hardware-supported lighting models assume that the viewer and light sources are positioned infinitely far from the object being illuminated. Although the positioning of the viewer and/or light sources at a finite distance from the object can enhance the realism of the scene, these models are often avoided because of costly inverse square root operations. The OCTANE geometry engines include special VLSI support for computing inverse square roots, thus speeding local lighting calculations enormously.

### 4.4.8 Atmospheric Effects

OCTANE graphics support fast per-pixel fog calculations in hardware. The fogging is done using 8-bits of precision. The fog value is then blended with the calculated color for the pixel based on span iteration.

The OpenGL Graphics Library API simulates those fog and haze effects required for visual simulation applications by blending the object color with a user-specified fog color. The user enjoys control over the fog density through the OpenGL Graphics Library interface. This functionality can also be used for depth cuing. With OCTANE, all fog functions (linear, exponential and exponential squared) can be used at the same level of performance.

### 4.4.9 Texture Mapping

#### 4.4.9.1 Motivation

OCTANE supports high speed hardware texture-mapping that is capable of generating images of the same high quality as those produced on high-end Silicon Graphics machines. Texture mapping has traditionally been used in fields such as visual simulation and computer animation to enhance scene realism.

#### 4.4.9.2 Quality

It is essential that errors be minimized during the texture-mapping process. Perspective correction of texture coordinates is performed during the scan-conversion process to prevent textures from “swimming” as an object moves in perspective. OCTANE supports perspective correction of one and two dimensional textures. Perspective correction and mipmapping of three dimensional (volume) textures was too expensive to implement in hardware and judged to be of limited utility in the applicable markets.

Texture aliasing is minimized by filtering the texture for each pixel textured. Without filtering, textures on surfaces appear to sparkle as surfaces move. Filtering is accomplished using an interpolation of the mip-maps in the TRAM. All core OpenGL 1.0 texture filtering modes are supported, including trilinear mipmapping. Quadrilinear filters for four dimensional textures

(only used for pixel texture color conversions) are possible by using multiple passes and alpha blending. Filtered representations of a texture are computed at different levels of resolution. OCTANE supports textures with one, two, three, or four components (luminance, luminance alpha, RGB, or RGBA) each having 4, 8, or 12-bits in depth. The texture mezzanine option is necessary to support some 8- and 12-bit texel modes that are not supported under the standard configuration, namely three and four component 8-bit texels and two, three and four component 12-bit texels.

OCTANE has the ability to define three 256-entry 8-bit texture color tables that can be applied to luminance or RGB textures after texture interpolation and filtering. These are of particular interest to markets like medical imaging where interactive contrast adjustment is necessary in viewing textured images and volumes.

#### 4.4.9.3 Flexibility

A variety of texture types and environments are provided to support the diverse applications of textures. Textures can be defined to repeat across a surface or to clamp outside of a texture's unit range. Textures can be in monochrome or color, and with or without alpha. Texture alpha can be used to make a polygon's opacity vary at each pixel. For instance, when an RGBA image of a tree is mapped onto a quadrilateral, objects behind the polygon can appear through the polygon wherever the opacity of the tree map is low, thereby creating the illusion of an actual tree.

Textures can be combined with their surfaces in a variety of ways. A monochrome texture can be used to blend between the surface color and a constant color to create effects such as grass on dirt or realistic asphalt. By adding alpha, a texture can be used to create translucent clouds. Textures can also be used to modulate the color of a surface, or be applied as a decal onto a surface.

The OCTANE architecture can automatically generate texture coordinates based on user-specified behavior. This feature can be used to texture map contours onto an object without requiring the user to compute or store texture coordinates for the object.

### 4.4.10 Stencil Planes

The eight independent stencil bit-planes implemented in the Raster Subsystem depth buffer provide a mechanism for affecting the results of pixel algorithms. In many ways, the stencil can be thought of as an independent, high-priority Z-buffer. The stencil value can be tested during each pixel write, and the result of the test determines both the resulting stencil value, and whether the pixel algorithm will produce any other result.

One application of the stencil is Z-buffered image copy. During the first pass, the stencil planes record the result of depth comparisons between source and destination areas of the frame buffer. During a second pass, the image is copied from source to destination, with only the pixels that passed the depth comparison being updated. As an example, this method can be employed with a library of small 3D images, such as spheres and rods, to quickly construct molecular models in the frame buffer.

A second application is the ability to draw hollow polygons. This technique is useful for visualizing the structure of solid models. By drawing the outline of each facet into the stencil,

and subsequently performing Z-Buffered drawings of the whole facet while using the stencil as a mask, the true joining edges of an object's surface can be displayed alone, highlighted, or with the background color filled to expose a hidden-line representation.

Most significantly, the stencil mechanism allows constructive solid geometry pixel algorithms to be implemented in a parallel environment. The flexible testing and updating constructs designed into the graphics engines allows the construction of unions and intersections of primitive shapes, all with the attributes of texture mapping, transparency, and anti-aliasing.

### 4.4.11 Arbitrary Clipping Planes

The Geometry subsystem supports the definition of six planes in 3D space. Geometric primitives can be clipped against these planes in addition to the normal six planes that describe the current viewing volume, providing an ideal mechanism for viewing the cross-section of model components or volumetric data.

Alternatively, the distance between a primitive and any plane can be calculated. This distance can be used as a texture-mapping coordinate which then can be used to produce a contour map applicable to any 3D model for improved visualization.

### 4.4.12 Pixel Read, Write, and Copy

OCTANE graphics offers a host of features that greatly enhance the pixel read, write, and copy operation. At the core of these features is a 64-bit DMA channel that provides ultra high-speed pixel transfers between the host and the frame buffer. In addition to the standard 32-bit pixel, various packed pixel formats are also supported, conserving system memory and bus bandwidth upon drawing. For applications interested in large data sets, pan and zoom are supported by the hardware at interactive rates.

For pixel reads or writes, the screen-relative direction of the read or fill (right-to-left or left-to-right, bottom-to-top or top-to-bottom) is user selectable. OCTANE also has dedicated hardware to support transfer and assembly of non-contiguous images (also called image tiling).

### 4.4.13 Imaging Operations

#### 4.4.13.1 Color Tables

Color tables are used to provide a one-dimensional look-up table per component, whether that component be intensity, luminance, red, green, blue or alpha. It is a more powerful mechanism than the pre-existing pixel map facility provided in the core OpenGL 1.0. While pixel map was restricted to mapping from a color index to RGBA or from RGBA to RGBA (both of which require four separate color look-up tables), the color table mechanism minimizes the amount of work to be done by allowing color look-ups on a subset of those components. For instance, you can map only luminance to luminance with color tables, requiring only one look-up per pixel. To do the same operation with a pixel map would require four times the amount of work. Color tables have applications in numerous markets including prepress, medical imaging, oil and gas visualization and GIS.

Color tables are accelerated and implemented in GE11 microcode. To ensure that they run as fast as possible, the number and size of the color tables for a given application should be reduced to an acceptable minimum.

#### 4.4.13.2 Convolutions

Convolutions are a generalized mechanism upon which many different imaging operations such as blurring, sharpening and edge detection can be implemented. A convolution is a spacial operation used to calculate what is going on with the pixel intensities around the point of processing. By taking information about the neighbors of the pixel being processed it is possible to calculate spacial frequency activity in the area and make discretionary decisions regarding the area's frequency content. This is achieved by making the output pixel brightness dependent on a group of pixels surrounding the center pixel in the input image. For every pixel in the input image, a value for the output image pixel is determined by calculating a weighted average of that pixel and its surrounding neighbors. The average is formed by placing the center of a square kernel (also known as a convolution mask or filter), which contains the weights or convolution coefficients, on the pixel being processed in the input image. The corresponding underlying pixels are then multiplied by the coefficients and the results are added to obtain the value of the output pixel. For example, in a typical convolution with a 3 x 3 kernel, nine multiplications and eight additions are required per pixel in the output image.

A kernel is defined per component or channel. The kernel, which can be thought of as a matrix, can be 3x3, 5x5 or 7x7 where each element is a floating point weight. The convolution operation is implemented in GE11 microcode. By increasing the kernel size, the flexibility of the filter is increased by taking into account more neighboring pixels. However, more processing is required and performance is reduced. Greater performance can be achieved by using separable convolutions. A convolution kernel is separable if it can be supplied as separate horizontal and vertical components. This allows the convolution to be performed sequentially in separate horizontal (rows) and vertical (columns) passes and greatly reduces the number of required multiplications and additions.

A post scale/bias operation is provided after the convolution to optionally alter the value of all output pixels by multiplying them by a common scale factor and adding a common bias.

#### 4.4.13.3 Color Matrix

Color Matrix provides the functionality for the RGBA components to be treated as a 4x1 vector and multiplied by a user-specified 4x4 matrix. This allows each component to be duplicated, eliminated, have its order switched with another component, or be linearly combined with other components. For example, linear color conversions such as HSV to RGB can be easily accomplished by using an appropriate matrix.

The matrix multiplication is implemented in GE11 microcode.

A post scale/bias operation is provided per component after the color matrix operation to optionally alter the value of all output pixels by multiplying them by a common scale factor and adding a common bias.

#### 4.4.13.4 Histogram

The Histogram operation counts the specific color components and provides a one-dimensional array (per component) containing the number of occurrences of each color component value in the input image. For best performance, the internal format of the histogram should match the external format of the image data in order to minimize unnecessary expansion and compression of the data.

The histogram operation is implemented in GE11 microcode. Histogram is one of the last operations performed in the pipeline so if the image data is no longer needed, it can be discarded once the histogram is calculated so that no drawing or texture loading will take place.

#### 4.4.13.5 Minmax

The Minmax operation scans the specific color components and provides a minimum and a maximum value for each color component of the input image. For best performance, the internal format of the Minmax should match the external format of the image data in order to minimize unnecessary expansion and compression of the data.

The Minmax operation is implemented in GE11 microcode. Minmax is one of the last operations performed in the pipeline so if the image data is no longer needed, it can be discarded once the minima and maxima are calculated so that no drawing or texture loading will take place.

### 4.4.14 Standard Visuals

The OCTANE frame buffer is based upon two types of fundamental building blocks: 36-bit buffers and 9-bit buffers. All supported visuals are some construction or combination of these. The desired screen resolution determines how many of each type of buffer may be used to construct a given visual. A great deal of flexibility is also given in determining the purpose of each buffer. For instance, each 36-bit buffer can take on the following identity (or use):

- 12/12/12 RGB color single buffer
- 8/8/8/8 RGBA color single buffer
- 5/5/5/1 RGBA color double buffer
- 4/4/4/4 RGBA color double buffer
- 12 color index double buffer
- 24-bit depth buffer and 8-bit stencil buffer (also called ZST)

Note that the total number of bits shown in each of buffer configurations above does not always equal 36, and that the 9-bit buffer has one bit “left over”. These extra bits are not wasted, but rather are used for identifying regions on the screen that require special interpretation upon pixel scan-out. An example would be two double buffered windows, where the displayed buffers can change independently. Additionally, some “extra” bits are used for very fast (or tagged) clears. The one case that completely utilizes all the bits for color (12/12/12 RGB) cannot take advantage of some of the these features, and will take somewhat longer to clear. Furthermore, a visual cannot be comprised of entirely 12/12/12 RGB buffers. An example

would be a 1280x1024 12/12/12/ RGB double buffered configuration. In this configuration there are no left over control bits to facilitate pixel interpretation and window clipping.

Some color buffers must be displayable. Those left over can be used as pbuffers.

Now that the building blocks have been explained, one needs to know how many are available on each OCTANE model at a given screen resolution. The 9-bit buffers are far less flexible than the 36-bit buffers and may only be used for an 8-bit color index overlay.

Table 4.2 OCTANE Buffers Available for Visuals

| Screen Resolution | High OCTANE | | Maximum OCTANE | |
|---|---|---|---|---|
| | 36-bit buffers | 9-bit buffers | 36-bit buffers | 9-bit buffers |
| 1024x768 | 3 | 1 | 6 | 1 |
| 1280x1024 | 2 | 1 | 4 | 1 |
| 1600x1200 | 1 | 1 | 2 | 1 |
| 1920x1035 HDTV | 1 | 1 | 2 | 1 |

Combinations of buffer configurations in the table above can result in the very large number of available visuals. Those visuals currently supported are shown in the Table 4.3 below. All visuals are available with or without a 64-bit software accumulation buffer.

Table 4.3 Available Visuals on OCTANE

| OCTANE Model | Screen Res | Type | Color Frame Buffer Bits | | | | Color Index Bits | Double Buffer Available | Stereo Available | Z-Buffer Bits | Stencil Buffer Bits | Vertical Refresh (Hz) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | R | G | B | A | | | | | | |
| SI/SSI | All | CI Ovly | | | | | 8 | No | No | 0 | 0 | 60,72,76 |
| SI/SSI | 1024x768 | CI | | | | | 8 | No | No | 24 | 8 | 60,72,76 |
| SI/SSI | 1024x768 | CI | | | | | 12 | No | No | 24 | 8 | 60,72,76 |
| SI/SSI | 1024x768 | CI | | | | | 12 | Yes | No | 24 | 8 | 60,72,76 |
| SI/SSI | 1024x768 | CI | | | | | 12 | Yes | Window | 24 | 8 | 96 |
| SI/SSI | 1024x768 | RGBA | 4 | 4 | 4 | 4 | N/A | Yes | No | 24 | 8 | 60,72,76 |
| SI/SSI | 1024x768 | RGBA | 4 | 4 | 4 | 4 | N/A | Yes | Window | 24 | 8 | 96 |
| SI/SSI | 1024x768 | RGBA | 5 | 5 | 5 | 1 | N/A | Yes | No | 24 | 8 | 60,72,76 |
| SI/SSI | 1024x768 | RGBA | 5 | 5 | 5 | 1 | N/A | Yes | Window | 24 | 8 | 96 |
| SI[1]/SSI | 1024x768 | RGBA | 8 | 8 | 8 | 8 | N/A | No | No | 24 | 8 | 60,72,76 |
| SI[1]/SSI | 1024x768 | RGBA | 8 | 8 | 8 | 8 | N/A | Yes | No | 24 | 8 | 60,72,76 |
| SI[1]/SSI | 1024x768 | RGBA | 12 | 12 | 12 | 0 | N/A | No | No | 24 | 8 | 60,72,76 |
| SI[1]/SSI | 1024x768 | RGBA | 12 | 12 | 12 | 0 | N/A | Yes | No | 24 | 8 | 60,72,76 |
| SI/SSI | 1280x960 | CI | | | | | 8 | No | No | 24 | 8 | 30 int. |
| SI/SSI | 1280x1024 | CI | | | | | 8 | No | No | 24 | 8 | 50,60,72,76 |
| SI/SSI | 1280x1024 | CI | | | | | 12 | No | No | 24 | 8 | 50,60,72,76 |
| SI/SSI | 1280x1024 | CI | | | | | 12 | Yes | No | 24 | 8 | 50,60,72,76 |
| SI/SSI | 1280x1024 | RGBA | 4 | 4 | 4 | 4 | N/A | Yes | No | 24 | 8 | 50,60,72,76 |
| SI/SSI | 1280x1024 | RGBA | 5 | 5 | 5 | 1 | N/A | Yes | No | 24 | 8 | 50,60,72,76 |
| SI[2] | 1280x1024 | RGBA | 8 | 8 | 8 | 0 | N/A | Yes | No | 0 | 8 | 50,60,72,76 |
| SI/SSI[2] | 1280x1024 | RGBA | 8 | 8 | 8 | 8 | N/A | No | No | 24 | 8 | 50,60,72,76 |
| SI | 1280x1024 | RGBA | 8 | 8 | 8 | 8 | N/A | Yes | No | 0 | 0 | 50,60,72,76 |
| SSI | 1280x1024 | RGBA | 8 | 8 | 8 | 8 | N/A | Yes | No | 24 | 8 | 50,60,72,76 |
| SI/SSI | 1280x1024 | RGBA | 12 | 12 | 12 | 0 | N/A | No | No | 24 | 8 | 50,60,72,76 |
| SSI | 1280x1024 | RGBA | 12 | 12 | 12 | 0 | N/A | Yes | No | 24 | 8 | 50,60,72,76 |
| SI/SSI | 1280x492 | CI | | | | | 8 | No | No | 0 | 0 | 120 |
| SI/SSI | 1280x492 | CI | | | | | 12 | No | No | 0 | 0 | 120 |

Table 4.3 Available Visuals on OCTANE (Continued)

| OCTANE Model | Screen Res | Type | Color Frame Buffer Bits | | | | Color Index Bits | Double Buffer Available | Stereo Available | Z-Buffer Bits | Stencil Buffer Bits | Vertical Refresh (Hz) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | R | G | B | A | | | | | | |
| SI/SSI | 1280x492 | CI | | | | | 12 | Yes | No | 0 | 0 | 120 |
| SI/SSI | 1280x492 | RGBA | 4 | 4 | 4 | 4 | N/A | Yes | Full | 24 | 8 | 120 |
| SI/SSI | 1280x492 | RGBA | 5 | 5 | 5 | 1 | N/A | Yes | Full | 24 | 8 | 120 |
| SI | 1280x492 | RGBA | 8 | 8 | 8 | 8 | N/A | No | Full | 24 | 8 | 120 |
| SSI | 1280x492 | RGBA | 8 | 8 | 8 | 8 | N/A | Yes | Full | 24 | 8 | 120 |
| SI | 1280x492 | RGBA | 12 | 12 | 12 | 0 | N/A | No | Full | 24 | 8 | 120 |
| SSI | 1280x492 | RGBA | 12 | 12 | 12 | 0 | N/A | Yes | Full | 24 | 8 | 120 |
| SSI[1] | 1600x1200 | RGBA | 4 | 4 | 4 | 4 | N/A | Yes | No | 24 | 8 | 72 |
| SI[1]/SSI[1] | 1600x1200 | CI | | | | | 8 | No | No | 0 | 0 | 60 |
| SI[1]/SSI[1] | 1600x1200 | CI | | | | | 12 | No | No | 0 | 0 | 60 |
| SI[1]/SSI[1] | 1600x1200 | CI | | | | | 12 | Yes | No | 0 | 0 | 60, |
| SI[1] | 1600x1200 | RGBA | 4 | 4 | 4 | 4 | N/A | Yes | No | 0 | 0 | 60 |
| SSI[1] | 1600x1200 | RGBA | 4 | 4 | 4 | 4 | N/A | Yes | No | 24 | 8 | 60 |
| SI[1] | 1600x1200 | RGBA | 5 | 5 | 5 | 1 | N/A | Yes | No | 0 | 0 | 60 |
| SSI[1] | 1600x1200 | RGBA | 5 | 5 | 5 | 1 | N/A | Yes | No | 24 | 8 | 60 |
| SI[1] | 1600x1200 | RGBA | 8 | 8 | 8 | 8 | N/A | No | No | 0 | 0 | 60 |
| SSI[1] | 1600x1200 | RGBA | 8 | 8 | 8 | 8 | N/A | No | No | 24 | 8 | 60 |
| SSI[1] | 1600x1200 | RGBA | 12 | 12 | 12 | 0 | N/A | No | No | 24 | 8 | 60 |
| SSI | 1920x1035 | RGBA | 12 | 12 | 12 | 0 | N/A | No | No | 24 | 8 | 60 (HDTV) |

[1] Available in patch 1105 for IRIX 5.3 and IRIX 6.2.
[2] These visuals can only be accessed by using setmon 1280x1024_xx_32db.

Full screen stereo visuals allow users to create high quality stereoscopic applications and display them with the aid of stereoscopic glasses. Stereo in a window allows the user the extra flexibility of displaying the application in the normal desktop environment. The OCTANE architecture supports stereo across the line, although the available resolutions and color depths depend on the amount of frame buffer available.

### 4.4.15 Detail Texture

The problem with ordinary texture mapping of objects is that at close range, the structure of the texture map becomes very apparent when the texels are magnified. However, providing a

texture map with sufficient detail to withstand very close visual scrutiny will frequently require more texture memory than could possibly be provided. To cope with this in certain situations, the concept of detail texturing was developed. Detail texturing allows the user to define two texture maps, the normal texture and a “detail texture”. When the user moves in past a certain LOD, the detail texture is used to modify the base texture. This can create the effect of revealing the underlying structure of a texture. For instance, one could use a detail texture on a texture map of a cloth to reveal the stitch pattern of the fabric rather than just the colors when zooming in. OCTANE supports additive detail texturing in hardware.

#### 4.4.16 Pixel Textures

Pixel texturing allows the OpenGL pixel path to be diverted and each pixel used as a look up into a four dimensional texture map. The process of performing this multi-dimensional look-up is performed for each pixel in the image. Each RGBA pixel is mapped to an equivalent texture coordinate STRQ, which is indexed into a four dimensional texture in texture memory. Non-linear color space conversions can be performed through pixel texturing, and by using OCTANE’s fast and sophisticated texture interpolation, the conversion will be highly accurate and can be accomplished at interactive rates. This will allow users to change CMYK to RGB and conversion parameters without having to wait for the results.

#### 4.4.17 Pixel Buffers

Pixel buffers or ‘pbuffers’ are a concept that has been requested for some time in OpenGL. They are off-screen rendering areas analogous to a GLXpixmap. Pixmaps are static and cannot use hardware acceleration. However, pbuffers can be volatile or nonvolatile and exist in framebuffer memory, thereby benefiting fully from hardware acceleration.

#### 4.4.18 Framebuffer Configuration (FBConfig)

This extension to OpenGL allows RGBA contexts to be bound to color index frame buffers, allowing the use of the powerful OpenGL RGBA rendering semantics with a color index visual. When converting to color index, the red channel is used for doing the look-up. Any other channels are ignored.

#### 4.4.19 Video Texturing

Several OpenGL extensions and the OCTANE architecture make the application of textures generated by video sources possible. OCTANE Compression or OCTANE Video can be given a straight path to texture memory. The TRAM’s ability to simultaneously load and render textures allows D1 video to be applied to geometry in real time. This is crucial for the film and video industry where page turns, complex wipes and other special effects can be implemented using texture mapping.

#### 4.4.20 Other OpenGL Extensions

The OCTANE system supports numerous OpenGL extensions. Refer to the *glIntro(1)* man page for a complete list of what is currently available and for a pointer to the individual man pages.

# *Section 5 Software Environment*

Silicon Graphics IRIX 6.4, known as Cellular IRIX, is the operating environment for the Octane system. IRIX 6.4 represents the initial release of Cellular IRIX, and introduces major improvements in scalability, compatibility, performance, throughput, and availability.

- Scalability - IRIX 6.4 can easily scale between the single and dual processor Octane configurations and is optimized for use with the multiprocessing features of the R10000 processor.
- Compatibility - IRIX 6.4 builds on the features, functions, and interfaces of the 64-bit IRIX 6.2 operating system.
- High Performance - IRIX 6.4 achieves high performance through innovative dynamic, explicit, and implicit data placement functionality.
- Throughput - Overall throughput is enhanced in IRIX 6.4 through the use of an advanced scheduler that insures fairness for interactive users.
- Availability - IRIX 6.4 provides increased levels of system availability over IRIX 6.2.

Each release of IRIX 6.4 contains a broad spectrum of useful multimedia applications:

- Digital Media Tools
- IRIS Showcase™
- InPerson™
- Mindshare™ OutBox
- Netscape Navigator™
- Netscape Mail™
- WebSpace Navigator™
- WebMagic™
- Adobe Acrobat™ Reader Version 2.1

## 5.1 Operating System

IRIX 6.4 is the Silicon Graphics implementation of the UNIX operating system, first developed by AT&T Bell Laboratories. IRIX 6.4 is based on AT&T UNIX System V.4, but also includes numerous 4.3 BSD extensions, such as TCP/IP network protocols and Network File System (NFS), which provide transparent access to files across a heterogeneous network. Adherence to these industry standards lets users easily integrate an Octane into existing computing environments.

In addition to the BSD extensions, IRIX 6.4 includes several enhancements to support the real-time requirements of 3D graphics and audio:

- Non-degrading priorities and high-resolution timers

- Kernel primitives and libraries that support multi-process applications and high-performance concurrent programming
- Memory-mapped files that allow a process to access a file as part of its address space
- A tight coupling between the operating system and OpenGL kernel routines to produce high graphics throughput

IRIX applications are binary compatible across the entire SGI product line, making it trivial to move existing applications to an Octane and to port applications developed on an Octane to other machines.

The IRIX 6.4 operating system offers a rich user and programming environment, and is compliant with the following window system and operating system standards:

- X11/R6
- IRIX/Motif, based on OSF/Motif Release 1.2.2
- Display PostScript
- AT&T UNIX System V.4, with 4.3 BSD enhancements
- POSIX 1003.1
- X/OPEN XPG3, Vol. 1,2,3

### 5.1.1 Scalability

IRIX 6.4 distributes previously shared kernel text into optimized ‘cells’. Processes running on these cells call, reference, and rely extensively on local operating system services, including local copies of operating system text. IRIX 6.4 manages global kernel data sharing across local cells with a distributed caching structure, preserving the familiar IRIX single system image while providing excellent hardware utilization.

### 5.1.2 Compatibility

IRIX 6.4 is compatible with the vast majority of IRIX 5.x and IRIX 6.x applications. Most of these applications run without modification. IRIX 6.4 uses the highly-functional user and developer interfaces from IRIX 6.2, while the administrative interfaces have been enhanced.

### 5.1.3 Availability

A new implementation of checkpoint-restart is an integral part of IRIX 6.4. With checkpoint-restart, administrators and privileged users can snap-shot a job in mid-execution with the capability to restart it later. Users with long-running jobs can regularly capture their progress, thereby protecting themselves against unexpected downtime events. The checkpoint-restart mechanism is kernel based and application transparent. Users can check existing binaries without modification.

### 5.1.4 Scheduler

The scheduler in IRIX 6.4 is optimized to support multi-processor applications and large numbers of user processes, making it ideal for use in a dual-processor Octane system.

Scheduler enhancements include process-to-memory affinity and currency-based space sharing for interactive users.

Traditional UNIX scheduling assigns a priority to each user. Newly spawned processes inherit the same priority. This degrades as the process runs to allow lower-priority processes an opportunity to run. With this scheme, a single-user with a relatively high priority can spawn a number of threads with the same priority and unfairly monopolize system resources. With the new IRIX 6.4, unfair monopolization of the system is much less likely.

Process-to-memory affinity allows the scheduler to interact with the new memory management subsystem in order to give short-term priority to processes and threads whose pages are still largely memory resident, as opposed to cache resident.

The currency-based space sharing features of the IRIX 6.4 scheduler changes the timesharing/ interactive job scheduling paradigm significantly, insuring long-term fairness for all users while enabling short term decision making for optimal application performance.

### 5.1.5 File Systems

IRIX 6.4 provides an advanced file system and supports a range of alternate file systems for distributed and standards-based data access. Some of these file systems include:

- File Services - The IRIX file subsystem supports multiple physical disks and gives them the appearance of a single, logical file system with a hierarchical arrangement.
- EFS - While support for EFS continues in IRIX 6.4, Silicon Graphics recommends conversion to XFS, one of the most advanced file systems available today. XFS is standard on IRIX 6.4.
- XFS - XFS is a 64-bit file system with a number of advanced features including very high throughput rates and guaranteed rate I/O. XFS uses database journaling technology to provide very fast file system recovery. No file system checking utility is required. The XFS system references a small log of recently updated file system transactions after a system crash. The XFS file system supports logical block sizes ranging from 512 bytes to 64 kilobytes. File system extents enable data contained in an extent to be placed on disk in contiguous file system blocks. The use of extents in XFS greatly increases I/O throughput by reducing disk seeks and rotational delays when data is read from or written to disk. The XFS guaranteed rate I/O option makes it the only file system that allows applications to reserve specific bandwidth to or from the file system. This functionality is valuable to applications that perform real-time data capture or delivery.
- NFS - Distributed file systems simplify the way data is accessed by making remote files appear local. NFS is the defacto UNIX standard for distributed file systems and comes standard on IRIX 6.4. To enhance file sharing performance and reduce network loading, NFS clients can use the Cache File System (CFS) function. CFS allows users to retain a local copy of frequently accessed remote files and update the cached copy only when the original has been changed. A Network Information System (NIS) is also provided for centralized file system management. The auto-mounter service automatically mounts and unmounts NFS file systems.
- ISO 9660 - This file system is used to mount CD-ROM discs in the High Sierra or ISO 9660 formats.

- DOS and Macintosh Floppies - IRIX 6.4 supports the industry standard single- and double-density, double-sided 3.5-inch floppy drive. Three 5.25-inch floppy formats are supported when used with a freestanding SCSI floppy drive. The 3.5-inch 20.1 MByte floptical drive is also supported, as are the HFS/MAC formats.

### 5.1.6 Memory Management

Memory management in IRIX 6.4 uses a sophisticated demand paging VM system designed to meet the challenges of a broad spectrum of applications. The VM system scales easily to accommodate very large physical memories, address spaces, and number of processes without sacrificing desktop performance. The IRIX 6.4 VM system includes the following features:

- Full support for SVR4 Application Programming Interface (API), including memory mapped files and devices.
- Full support for SVR4 MIPS Application Binary Interface (ABI).
- 64-bit user virtual addresses, allowing individual processes with address spaces spanning terabytes.
- Dynamic loading of libraries.
- Efficient process creation by using lazy replication of data pages (copy-on-write).
- Efficient support for parallel programming by sharing address space between multiple processes of threads.
- Multiple swap devices, including swapping to regular files in local or remote NFS file systems.
- Multiple page sizes within a single process address space. In processors that support multiple page sizes, such as the R10000 processor in the Octane system, the VM system allows a program to request that specific ranges of its address space be represented using pages that are multiples of the base page size. This allows programs with large data sets and poor spatial reference locality to minimize address Translation Lookaside Buffer (TLB) overhead.
- Automatic replications of shared text pages.
- Automatic migration of shared data pages.

## 5.2 Development Tools

Silicon Graphics provides a broad range of standard and optional graphics and visualization development tools.

For window management, the Octane system provides a full implementation of the X11/R6 Window System, Display PostScript™, and 4Dwm™, a Motif™-based window manager. To resolve any potential color conflicts between X11 and 3D graphics applications, Octane keeps completely separate color maps for both X11 and OpenGL applications.

For image processing on Octane, the Silicon Graphics ImageVision Library™ offers an object-oriented extensible toolkit for creating, processing, and displaying images. A core set of over 70 routines provides general purpose image operators which are easily augmented using abstract data types (objects) and access functions (methods). It also provides a general interface for image-processing applications, support for SGI, TIFF, and FIT formats, an

optimal memory model for handling large images, and an architecture that supports general image types.

### 5.2.1 IRIX/Motif

The Octane system supports both X11 Window System Release 6 for both client and server, and IRIX IM, the Silicon Graphics enhanced version of OSF Motif 1.2.4. The X11 libraries have been updated to support 32-bit and 64-bit addressing. In addition, the Octane system also provides support for CID keyed fonts, the X double-buffering extension, and enhanced font installation and management.

### 5.2.2 Display PostScript

The Display PostScript (DPS) server from Adobe is shipped as part of the IRIX 6.4 window system. The DPS library is included as part of the Graphics Development Option for Octane, and can be used in conjunction with X and Motif to create complete 2D applications.

### 5.2.3 X11 and the OpenGL

The Silicon Graphics implementation of X11/R6 fully supports GLX, the Open GL extension to the X Window System.

### 5.2.4 OpenGL

OpenGL is a cross-platform, portable Application Programming Interface (API). OpenGL allows 2D, 3D, and imaging applications to be developed only once for deployment across a wide variety of hardware platforms with different operating systems and windowing environments.

OpenGL offers over 300 function calls available in C, C++, Fortran77, Ada, and Pascal versions. It supports input devices such as the mouse and keyboard, digitizing tablets, dial and button boxes, and the spaceball. When used in conjunction with a toolkit like IRIX/Motif, the OpenGL lets developers create highly responsive graphics applications with industry-standard user interfaces.

OpenGL programmers define object, world, and viewing coordinate systems, and apply orthographic or perspective projections to map them to any viewport on the screen. Objects can be translated, rotated, and scaled in real time, without flicker, by taking advantage of high-speed OpenGL 3D rendering capabilities and double buffering. OpenGL includes powerful primitives that allow programmers to create points, lines, arcs, circles, polygons, parametric curves, rational bi-cubic patches, and Gouraud shaded, Z-buffered solids. Complex objects can be quickly built by combining these primitives.

### 5.2.5 Open Inventor

The Silicon Graphics Open Inventor library uses an object-oriented approach to make the creation of interactive 3D graphics applications as easy as possible. Open Inventor presents a programming model based on a 3D scene database that dramatically simplifies graphics

programming. Open Inventor offers a rich set of objects that shortens programming time and extends 3D programming capabilities beyond OpenGL, X11, and Motif. Open Inventor provides prepackaged tools for viewing, manipulating, and animating 3D objects.

### 5.2.6 IrisGL™ on OCTANE

IGLOO (IrisGLOnOpen) is a version of IrisGL designed to run on top of OpenGL. It is provided for new graphics products that have a native implementation of OpenGL, but limited native support for IrisGL. Not all primitives map one-to-one from IrisGL to OpenGL, and some IrisGL calls run slower in IGLOO via a software implementation of the function. Other IrisGL calls that are obsolete may not be supported at all; they will have a stub in the library which executes a no-op. IMPACT offers native hardware support for key IrisGL primitives so that reasonable performance can be achieved, but OpenGL applications have a noticeable performance advantage over IrisGL applications. Developers are strongly encouraged to port their applications to OpenGL.

Compiling on IrisGL is the same as with previous 5.x releases, and the executable will access the objects in libgl.so. There is no need to recompile binaries that were previously compiled on 5.x software; however, binaries compiled on 4.0.5 or earlier software must be recompiled for best performance under IGLOO. Programs compiled on 4.0.5 (or earlier) generate binaries in the COFF file format, and they are incompatible with the ELF format binaries that are generated when compiling with 5.0 or later system software.

### 5.2.7 CASEVision

CASEVision™ is a visual processing technology that provides an advanced, interactive, visual development environment. CASEVision brings the advantages of visualization to software developers by providing the ability to see processes and data structures.

The ToolTalk integration mechanism allows both Silicon Graphics and third-party solutions to be tightly integrated so users can concentrate on the job at hand instead of managing the boundaries between the individual tools. The CASEVision environment is optional and composed of the following major components:

- CASEVision/Workshop is an Interactive programming environment that consists of a Static Analyzer, a visual Debugger, a Performance Analyzer and a Build Analyzer.
- CASEVision/ClearCase is an advanced Configuration Management, Version Control and Build Management system designed to support large-scale development.
- CASEVision/Tracker is a flexible event tracking system that is tightly integrated with other CASEVision solutions.

### 5.2.8 Compilers and Standard Development Tools

Silicon Graphics supplies a variety of compilers, such as ANSI standard C and Power C, Fortran and Power Fortran, C++, Ada, and Pascal.

IRIX 6.4 includes a set of profiling tools that can identify CPU-intensive code fragments to help focus optimization efforts. Prof and pixie provide detailed analyses of application

performance. Grosview gives a view of system loading; users can see what percentages of the available CPU, I/O, and other resources are being used at any given time.

IRIX 6.4 also includes general and specialized debuggers. Dbx, a standard UNIX source-level debugger is included. In addition, IRIX 6.4 comes with *gldebug*, specifically designed for debugging graphics applications created using the IRIS Graphics Library (IrisGL). It includes a viewer which graphically displays the state of the IrisGL as the application is running, and a controller, which lets the user interactively set break points and change the level of debugging output.

### 5.2.9 Image Processing Library

The ImageVision Library™ object-oriented extensible toolkit is used for creating, processing, and displaying images on the Octane system. The toolkit provides a framework for managing and manipulating images to aid image processing application developers. The Image Vision Library end-user environment is bundled with IRIX 6.4. Some of the features are:

- A core set of general purpose image operators and an easy way to add new operators. The first release contains a core set of about 70 routines. A set of abstract data types (objects) and access functions (methods) are provided to allow a developer to design and augment the set of image operators.
- Support for three standard image formats: SGI, TIFF, and a tiled format based on TIFF called FIT. New file formats can be seamlessly integrated into the library as needed.
- An optimal memory model for handling large images. ImageVision Library provides a memory model for efficient manipulation of general image data types, sizes, and resolutions. It includes a configurable cache to allow access to and processing of very large images.
- An architecture that supports general image types. ImageVision Library provides an interface for manipulating image attributes and image data that requires little or no knowledge of the internal structure and format of the image.

### 5.2.10 Digital Media Libraries

Several libraries are available for Octane workstations that assist programmers in developing multimedia applications incorporating 2D and 3D graphics and audio, and provide support for video I/O devices. Key among these are the Audio Library, the IndigoVideo Library, the MIDI Library and Compression Library, and the Image Processing Library.

The Digital Media Development Option offers a comprehensive and intelligent environment for digital media application development on the Octane Workstation. Six library modules, which can be called from C and C++, enable the rapid development of audio, video and MIDI applications.

The Audio Library and Audio File Library access the basic capabilities: reading and writing samples from the hardware and reading and writing disk files in AIFF and AIFF-C formats. The CD-ROM Audio Library and DAT Audio Library provide transport control and access the audio capabilities of the optional CD-ROM and DAT drives. The MIDI Library supports reading and writing of time-stamped MIDI messages through Octane serial ports using a

Macintosh® serial port to MIDI converter. It also assists with the parsing of incoming MIDI messages.

### 5.2.11 IRIS Performer

The IRIS Performer™ application development environment from Silicon Graphics automatically optimizes graphical applications on the full range of Silicon Graphics systems without changes or recompilation. IRIS Performer allows developers the means to achieve a fast, consistent frame rate for applications such as visual simulation, interactive entertainment, and simulation-based design. The IRIS Performer libraries are highly tuned for the Octane system and build on the foundations of OpenGL and IRIX 6.4. Key developer benefits include simplified management of the visual database and maximum performance for scene rendering on all Silicon Graphics workstations.

## 5.3 Indigo Magic™

Indigo Magic is an enhanced Silicon Graphics desktop interface for visual computing. Indigo Magic is now fully integrated into the World Wide Web and offers far more benefits than generic common desktop interfaces. The icons provide a visual interface to file system navigation, mounting of remote devices, searching for resources on the network—every aspect of interacting with UNIX. Icons are used to represent files, applications, people, machines, devices, etc., and they change in appearance to indicate a state of activity. A printer icon, for example, changes its appearance to indicate when the printer software is processing a document or when the printer is idle.

Indigo Magic lets you create multiple desktops containing all of the applications, files, and tools required for specific projects. The desktops can also be organized by functions; for example, creating one desktop for software development and another for computer aided design.

Indigo Magic is implemented using the enhanced version of the Motif toolkit rendered using the X-Window System. This integrated environment includes:

- Icons on background for applications, documents, and remote/local devices.
- Icon views allow browsing and copying from HTTP and FTP sites, as well as from directories.
- Built-in Media Viewers for HTTP, movie text, sound, and VRML documents.
- The ability to publish documents from your desktop to an automatically created home page.
- Task-based graphical personal administration tool, including modem support.
- Searchable web-based documentation and help delivery.
- Window overview/multiple desks for reducing screen clutter.
- Proactive system monitoring to alert the user of potential system problems.
- Bundled multimedia, collaborative, and web-based tools.
- Built-in access to Mac/PC file systems, including accessing floppies in both formats.
- SoftWindows for accessing PC applications and documents.

### 5.3.1 IRIS InSight™ Viewer

Now you can access Silicon Graphics end user manuals, customer support, and product information directly on your workstation using IRIS InSight Viewer. Remarkably easy to use, IRIS InSight Viewer offers fast access to online documents. IRIS InSight Viewer and Document Library are shipped with all new graphics systems. Online manuals can be accessed from a system disk, a server, or directly from CD-ROM.

### 5.3.2 IRIS Showcase™ 3.3

IRIS Showcase™ 3.3 allows you to create interactive documents that incorporate text, raster images, digital audio, live video graphics, and 3D objects. A Showcase document can be viewed as an interactive presentation or an onscreen slide show, captured on video tape for a video presentation, printed as a paper document or overhead, or encoded as ASCII and sent as an email message.

Showcase 3.3 allows you to create, import, and edit Inventor-based 3D models. The primary application can be used to develop model data and then import the data into Showcase to take advantage of the editing and interactive presentation features. 3D editing capabilities include:

- Material editor
- Material palette
- Texture editor
- Extrusion profile editor
- Light and shadow editor

Translators to the Inventor file format for DXF, IGES, and several applications are available.

Showcase HyperScripts allow you to create interactive documents that include scripted actions linked to objects on a page. HyperScript actions include page turns, launching other applications, playing video, playing audio and many others.

Showcase also supports a wide selection of font families and point sizes. Fonts can be rotated, scaled interactively, and converted to 2D graphics.

### 5.3.3 Media Tools

Indigo Magic includes a set of powerful easy-to-use tools providing basic production capabilities for a range of media. There are tools to capture, create, and manipulate standard-format images, with support for image scan, blur, rotate, scale, stretch, sharpen, and more. The video tools provide plug and play capability with NTSC or PAL video input and output. Users can grab video frames, create and edit movies, and create audio annotation. A Video Control Panel, Video Pro Panel, Movie Maker, Movie player, Audio Control Panel, SoundEditor and SoundFiler, CD Manager and DAT Manager are included with the Indigo Magic media tools. In addition, Indigo Magic Movie Tools support creation and playback of QuickTime™ movies as well as a Silicon Graphics movie format.

### 5.3.4 Digital Media Clip Library

With over 20 MB of ready-to-use images, sounds, movies and 3D objects, the Digital Media Clip Library takes you several steps closer to compelling interactive presentations.

## 5.4 Networking

Silicon Graphics offers a complete set of high-performance networking products with the fastest IP connectivity in the industry. IRIX 6.4 provides TCP/IP and a complete suite of Internet and BSD network application programs. For administering medium to large networks, Silicon Graphics' offers NetVisualyzer™, which allows the user to interactively locate and correct network bottlenecks and breakdowns, and to analyze network usage via graphical displays of the entire network.

Octane workstations connect out of the box to Ethernet networks. In addition, several optional networking products are currently available:

- NFS™ with the Network Information System™ (NIS) allows file sharing, directory services, and data format interpretation.
- TCP 3270 software allows Octane workstations to connect to an IBM mainframe via Ethernet.
- SNA 3270, 3770, and LU6.2 software allows Octane workstations to connect to an IBM mainframe through an SNA gateway.
- 4DDN software allows Octane workstations to connect to a DEC system using DECnet™ protocols.
- Macintosh connectivity (third party solution)
- SNMP agent
- Distributed IRIS GL
- NetVisualyzer (visual traffic monitor)

The networking capabilities of an Octane workstation can also be expanded with the addition of an optional FDDI port.

# *Section 6 Specifications*

This section lists the hardware specifications of the OCTANE system, including physical dimensions, connector drawings and corresponding connector pinouts for each port.

## 6.1 OCTANE Ports

The OCTANE system contains the following ports:

- Audio ports
  - microphone
  - speaker
  - analog line level audio
  - coaxial digital audio
  - optical digital audio
- SCSI Port
- Ethernet 10 Base-T/100 Base-T Port
- Parallel Port
- Keyboard and Mouse Ports
- Serial Ports
- Monitor Port
- Stereo View Port

### 6.1.1 Audio Ports

The OCTANE audio system contains the five ports shown above. Each port is explained in the following sections.

#### 6.1.1.1 Microphone Port

Table 6.1 shows a diagram of a microphone jack interfacing to the microphone port on the OCTANE system.

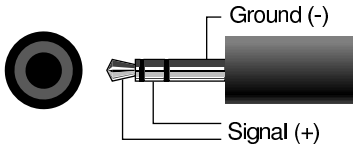


Figure 6.1 Microphone Port

Table 6.1 shows the microphone port pinout.

Table 6.1 Microphone Port Pinout

| Microphone | Tip | Ring | Sleeve |
|---|---|---|---|
| Silicon Graphics supplied electret mono microphone | Signal(+) | Signal(+)<br>NC (no connection) | Ground(-) |
| Line level mono microphone | Ground (-) | Signal (+) | Ground (-) |

#### 6.1.1.2 Speaker Port Pinout

Figure 6.2 shows a diagram of a speakerphone jack interfacing to the speakerphone port on the OCTANE system.

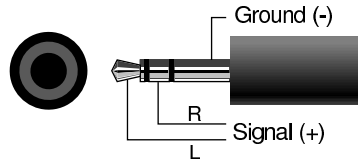


Figure 6.2 Speakerphone Port

Table 6.2 shows the sp4eakerphone port pinout.

Table 6.2 Speaker/Headphone Port Pinout

| Tip | Ring | Sleeve |
|---|---|---|
| Left Channel | Right Channel | Ground |

Figure 6.3 shows a diagram of the speakerphone power plug interfacing to the speakerphone power port on the OCTANE system.

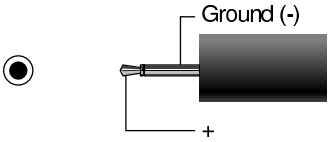


Figure 6.3 Speakerphone Power Plug

Table 6.3 shows the speaker power port pinout.

Table 6.3 Speaker Power Port Pinout

| Speaker | Tip | Sleeve |
|---|---|---|
| 10 Volt DC<br>500 mA | Power (+) | Ground |

#### 6.1.1.3 Analog Line Level Port Pinout

The OCTANE system contains four analog jacks, two input and two output. The jacks are color-coded, with red indicating the right channel, and white indicating the left channel. Figure 6.4 shows right and left analog jacks interfacing to the analog audio port on the OCTANE system.

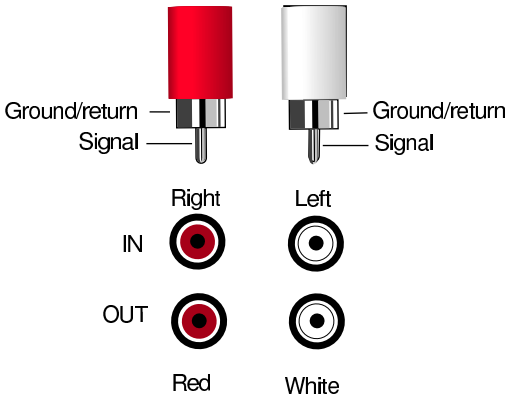


Figure 6.4 Analog Audio Port

#### 6.1.1.4 Coaxial Digital Port Pinout

The OCTANE system provides a coaxial digital audio port used for interfacing to audio components that support digital signals. The jacks are color-coded, with red indicating the right channel, and white indicating the left channel.

The coaxial digital audio interface supports the AES3id professional format and is compatible with consumer formats including CP340, IEC958, and S/PDIF.

Figure 6.5 shows the right and left coaxial digital jacks interfacing to the coaxial digital audio port on the OCTANE system.

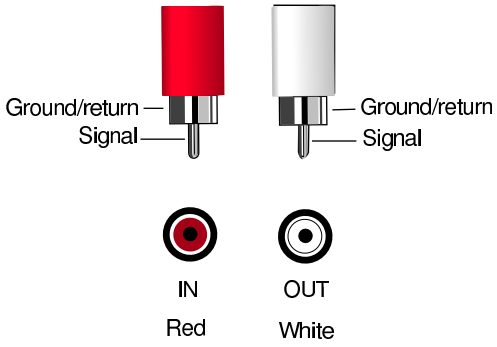


Figure 6.5 Coaxial Digital Audio Port

#### 6.1.1.5 Optical Digital Port Pinout

The OCTANE system provides an ADAT optical digital audio port used for interfacing to audio components that support the ADAT optical digital format.

The 2-channel (stereo) connection is fundamentally the same signal as described above in the section on coaxial digital audio. All aspects of the actual signal waveform are the same; the only difference is that this ADAT signal is carried on multimode plastic fiber optical material instead of copper wire. The fiber-optic stereo connection is compatible with consumer products such as DAT decks and CD players.

The ADAT optical interface supports ADAT 8-channel, 24-bit connections and is compatible with consumer formats including CP340, IEC958, and S/PDIF.

Figure 6.6 shows the right and left optical digital audio jacks interfacing to the optical digital audio port on the OCTANE system.

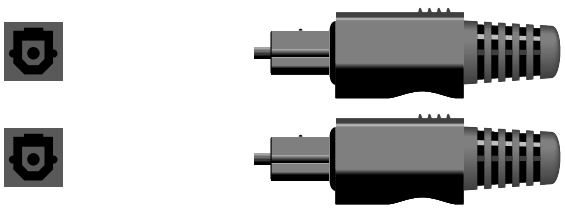

Figure 6.6 ADAT Optical Digital Audio Port

### 6.1.2 SCSI Port

The OCTANE system provides a SCSI port for interfacing to peripheral components such as external disk drives, CD-ROM, tape drive, etc. Figure 6.7 shows a diagram of the SCSI connector.

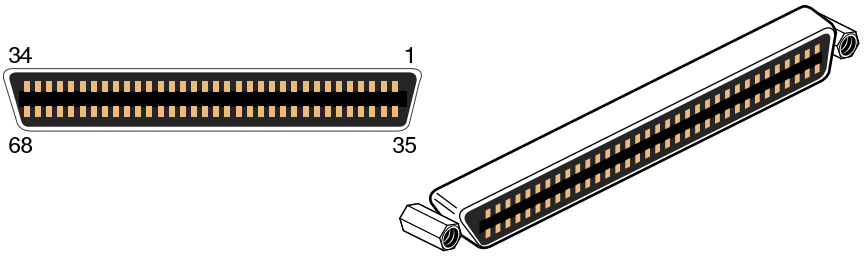


Figure 6.7 SCSI Port Connector

Table 6.4 shows the cable pinout assignments for the SCSI port.

Table 6.4 SCSI Port Pinout

| Pin | Assignment | Pin | Assignment |
|---|---|---|---|
| 1 | Ground | 35 | DB(12) |
| 2 | Ground | 36 | DB(13) |
| 3 | Ground | 37 | DB(14) |
| 4 | Ground | 38 | DB(15) |
| 5 | Ground | 39 | DB(P1) |
| 6 | Ground | 40 | DB(0) |
| 7 | Ground | 41 | DB(1) |
| 8 | Ground | 42 | DB(2) |
| 9 | Ground | 43 | DB(3) |
| 10 | Ground | 44 | DB(4) |
| 11 | Ground | 45 | DB(5) |
| 12 | Ground | 46 | DB(6) |
| 13 | Ground | 47 | DB(7) |
| 14 | Ground | 48 | DB(P) |
| 15 | Ground | 49 | Ground |
| 16 | Ground | 50 | Ground |
| 17 | Termpwr | 51 | Termpwr |
| 18 | Termpwr | 52 | Termpwr |
| 19 | Open | 53 | Open |
| 20 | Ground | 54 | Ground |

Table 6.4 SCSI Port Pinout (Continued)

| Pin | Assignment | Pin | Assignment |
|---|---|---|---|
| 21 | Ground | 55 | ATN |
| 22 | Ground | 56 | Ground |
| 23 | Ground | 57 | BSY |
| 24 | Ground | 58 | ACK |
| 25 | Ground | 59 | RST |
| 26 | Ground | 60 | MSG |
| 27 | Ground | 61 | SEL |
| 28 | Ground | 62 | C/D |
| 29 | Ground | 63 | REQ |
| 30 | Ground | 64 | I/O |
| 31 | Ground | 65 | DB(8) |
| 32 | Ground | 66 | DB(9) |
| 33 | Ground | 67 | DB(10) |
| 34 | Ground | 68 | DB(11) |

### 6.1.3 Ethernet 10 Base-T/100 Base-T Port

The OCTANE system contains an Ethernet port that supports both 10 Base-T and 100 Base-T transfer protocols. The port uses a form of auto-negotiation to select the speed (10 MBits/s, 100 MBits/s) and type (duplex vs. half duplex) at power-up. Figure 6.8 shows a diagram of the Ethernet port connector.

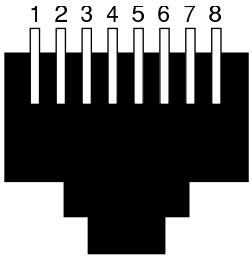


Figure 6.8 Ethernet Port

Table 6.5 shows the cable pinout assignments for the Ethernet 10 Base-T/100 Base-T port.

Table 6.5 Ethernet 10 BASE-T/100 BASE-T Port Pinout

| Pin | Assignment |
|---|---|
| 1 | Transmit+ |
| 2 | Transmit– |
| 3 | Receive+ |
| 4 | (Reserved) |
| 5 | (Reserved) |
| 6 | Receive– |
| 7 | (Reserved) |
| 8 | (Reserved) |

### 6.1.4 Parallel Port

The OCTANE system provides a 36-pin parallel port for interfacing to parallel devices such as printers, external removable hard drives, etc. Figure 6.9 shows a diagram of the parallel port connector.

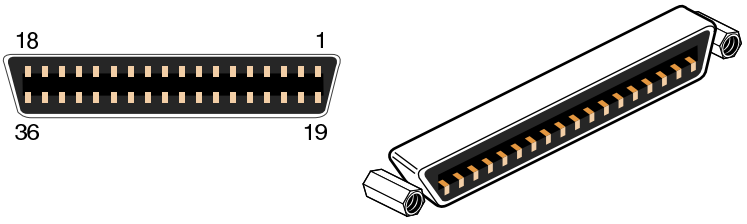


Figure 6.9 Parallel Port

Table 6.6 shows the cable pinout assignments for the parallel port.

Table 6.6 Parallel Port Pinout

| Pin | Assignment | Pin | Assignment |
|---|---|---|---|
| 1 | BUSY | 19 | Signal Ground (BUSY) |
| 2 | SELECT | 20 | Signal Ground (SELECT) |
| 3 | nACK | 21 | Signal Ground (nACK) |
| 4 | nFAULT | 22 | Signal Ground (nFAULT) |

Table 6.6 Parallel Port Pinout (Continued)

| Pin | Assignment | Pin | Assignment |
|---|---|---|---|
| 5 | pERROR | 23 | Signal Ground (pERROR) |
| 6 | DATA 1 | 24 | Signal Ground (DATA 1) |
| 7 | DATA 2 | 25 | Signal Ground (DATA 2) |
| 8 | DATA 3 | 26 | Signal Ground (DATA 3) |
| 9 | DATA 4 | 27 | Signal Ground (DATA 4) |
| 10 | DATA 5 | 28 | Signal Ground (DATA 5) |
| 11 | DATA 6 | 29 | Signal Ground (DATA 6) |
| 12 | DATA 7 | 30 | Signal Ground (DATA 7) |
| 13 | DATA 8 | 31 | Signal Ground (DATA 8) |
| 14 | nINIT | 32 | Signal Ground (nINIT) |
| 15 | nSTROBE | 33 | Signal Ground (nSTROBE) |
| 16 | nSELECTIN | 34 | Signal Ground (nSELECTIN) |
| 17 | nAUTOFD | 35 | Signal Ground (nAUTOFD) |
| 18 | HOST LOGIC HIGH | 36 view | PERIPHERAL LOGIC HIGH |

### 6.1.5 Keyboard and Mouse Ports

The OCTANE system provides two standard 6-pin mini-DIN connector for interfacing to a PS/2®-compatible keyboard and mouse. The ports are identical and interchangeable. Each port can be connected to either the mouse or the keyboard. An on-board auto-detection mechanism determines which peripheral is connected. Figure 6.10 shows a diagram of the keyboard and mouse ports

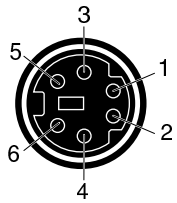


Figure 6.10 Keyboard and Mouse Port

Table 6.7 shows the keyboard and mouse port pinout.

Table 6.7 Keyboard and Mouse Port Pinout

| Pin | Assignment |
|---|---|
| 1 | Keyboard/Mouse Data |
| 2 | (Reserved) |
| 3 | Ground |
| 4 | Keyboard/Mouse Power (+5V) |
| 5 | Keyboard/Mouse Clock |
| 6 | (Reserved) |

### 6.1.6 Serial Ports

The OCTANE system provides two DB9 serial ports. Both ports contain male connectors as shown in Figure 6.11 below. The serial ports can operate in one of several modes:

- RS-232 electrical levels with a standard PC pinout.
- Macintosh-style electrical levels with a Macintosh-compatible pinout. This mode requires an additional adapter cable.
- ANSI/SMPTE 207M electrical levels and pinout. This mode requires an additional adapter cable.

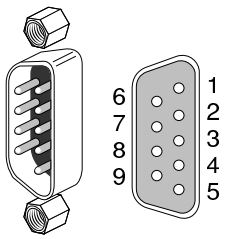


Figure 6.11 Serial Ports

Table 6.8 shows the pinout assignments for the serial ports in PC-compatible mode. The range of supported baud rates is 300 baud to 460K baud.

Table 6.8 Serial Port Pinout - PC-Compatible

| Pin | Assignment | Description |
|---|---|---|
| 1 | DCD | Data Carrier Detect |
| 2 | RD | Receive Data |
| 3 | TD | Transmit Data |
| 4 | DTR | Data Terminal Ready |
| 5 | SG | Signal Ground |
| 6 | DSR | Data Set Ready |
| 7 | RTS | Request to Send |
| 8 | CTS | Clear to Send |
| 9 | RI | Ring Indicator |

Table 6.9 shows cable pinout assignments for the serial ports in Macintosh-compatible mode.

Table 6.9 Serial Port Pinout - Macintosh-Compatible

| Pin | Assignment | Description |
|---|---|---|
| 1 | GPi | General Purpose Input |
| 2 | RxD- | Receive Data- |
| 3 | TxD- | Transmit Data - |
| 4 | TxD+ | Transmit Data + |
| 5 | SG | Signal Ground |
| 6 | RxD+ | Receive Data + |
| 7 | HSKo | Handshake Out |
| 8 | HSKi | Handshake In |
| 9 | Unused | |

## 6.2 Ports on XIO Graphics Boards

### 6.2.1 Monitor Port

The monitor port is included on all OCTANE graphics boards. The port consists of three coaxial connectors for the Red, Green, and Blue (RGB) video signals, as well as ten additional pins for synchronization, control and feedback. Figure 6.12 shows a diagram of the monitor port connector.

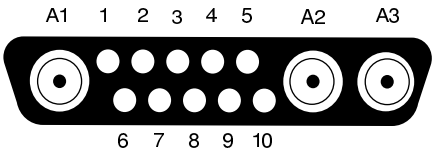


Figure 6.12 Monitor Port

Table 6.10 shows the pinout assignments for the OCTANE monitor port.

Table 6.10 Monitor Pinout

| Pin | Assignment |
|---|---|
| A1 | Red Signal, Analog |
| A2 | Green Signal, Analog |
| A3 | Blue Signal, analog |
| 1 | Monitor ID Bit 3, TTL |
| 2 | Monitor ID Bit 0, TTL |
| 3 | Composite Sync (Active Low), TTL |
| 4 | Horizontal Drive (Active High), TTL |
| 5 | Vertical Drive (Active High), TTL |
| 6 | Monitor ID Bit 1, TTL |
| 7 | Monitor ID Bit 2, TTL |
| 8 | Ground |
| 9 | Ground |
| 10 | Ground |

### 6.2.2 Stereo View Port

The OCTANE system provides one female DB9 stereo view port for synchronization to stereo goggles. The port connects to a transmitter that sits atop the OCTANE system. The transmitter transmits signals to the goggles being worn by the user, providing for a 3D stereo image. Figure 6.13 shows a diagram of the stereo view port connector.

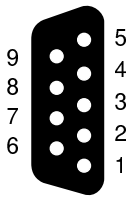


Figure 6.13 Stereo View Port

Table 6.11 shows the stereo view port pinout assignments.

Table 6.11 Stereo View Pinout Assignments

| Pin | Assignment |
|---|---|
| 1 | Stereo left/right Eye Signal (1=left, 0=right) (STEREO_LEFT) |
| 2 | Signal Return Ground |
| 3 | Reserved for Future Use |
| 4 | Signal Return Ground (Framelock ground) |
| 5 | Reserved for Future Use (Framelock) |
| 6 | Digital Return Ground |
| 7 | Digital Return Ground for Stereo View |
| 8 | +12V DC Output to Stereo View Device |
| 9 | Unused |

### 6.3 Physical Environment Specifications

Table 6.12 shows the physical environment specifications for the OCTANE system.

Table 6.12 Physical Environment Specifications

| Parameter | Type |
|---|---|
| Workstation dimensions | 16.25” (41.3 cm) H x 11.0” (28 cm) W x 13.25” (33.7 cm) D<br>14.75” D (37.5 cm) (depth in localized area of power supply)<br>16.25” D (41.3 cm) (depth in localized area of optional PCI module) |
| Power Requirements | Voltage and frequency: 100-240 VAC, 50-60 Hz, 10-4.2A, 850W |
| Ambient Temperature | +13° C (23.4° F) to +35° C (95° F) (operating)<br>-10° C (14° F) to +65° C (149° F) (non-operating) |
| Relative Humidity | 10% to 80% operating (no condensation)<br>10% to 95% non-operating (no condensation) |
| Heat Dissipation | 700 watts, 2400 Btu/hr |
| Altitude | 10,000 ft. (3,049 m) operating;<br>40,000 ft. (12,195 m) non-operating |
| Vibration | 0.02’, 5-19Hz; 0.35 G, 19-500 Hz |
| Voltage and frequency | 100-120/200-240 VAC |

### 6.4 Microphone Specifications

Table 6.13 shows the microphone specifications.

Table 6.13 Microphone Specifications

| Parameter | Type |
|---|---|
| Connector | 3.5 mm stereo mini |
| Power | +5 V phantom power on tip |
| Type | Unidirectional electret condenser |

### 6.5 Speaker Specifications

Table 6.14 shows speaker specifications.

Table 6.14 Speaker Specifications

| Parameter | Type |
|---|---|
| Rated power | 3 W(average) per channel |
| Frequency range | 180 Hz - 15K Hz |
| Magnetic flux leakage | <50 mGauss @2 cm |
| Input impedance | 150 ohms |
| Signal connector | 3.5 mm stereo mini |
| Power connector | 2.5 mm mono micro |

### 6.6 Headphone Specifications

Table 6.15 shows headphone specifications.

Table 6.15 Headphone Specifications

| Headphones | Type |
|---|---|
| Recommended impedance | 35 ohms |
| Connectors | 3.5 mm stereo mini |

### 6.7 Analog Line Level Audio Specifications

Table 6.16 provides the analog audio line level specifications.

Table 6.16 Analog Line Level Specifications

| Parameter | Line In | Line Out |
|---|---|---|
| Line level | -10dBV | -10dBV |
| 0dBFS Maximum | +10dBV to -22dBV | 6.5dBV ± 0.5dBV |

### 6.8 PCI Module Power Specification

Total power for the PCI module (the sum of power for all boards from all power supply rails) must not exceed 45.0W (average 15.0W per board).

The OCTANE PCI module is a 5V system environment.

Table 6.17 PCI Module Power Specifications

| Power Supply Rail | Maximum Current | Maximum Power |
|---|---|---|
| 3.3V | 10.0A | 33.0W |
| 5.0V | 9.0A | 45.0W |
| 12.0V | 1.5A | 12.0W |
| -12.0V | 0.3A | 3.6W |

# *Section 7 Standard OCTANE Configurations*

OCTANE provides an unprecedented amount of bandwidth, compute power and graphics quality in a desktop system. Even those working with extremely complex and large data sets can attain a level of interactivity and responsiveness previously limited to high end systems. Leading software developers for demanding industries, including manufacturing, entertainment, defense and science, have optimized their software to take full advantage of the functionality that the OCTANE system offers. The flexibility and scalability of the system make it the ideal choice for accommodating future needs and technological advances that may be in store.

OCTANE is equipped to work in any computing environment. Built-in adapters lower the cost of common connections. OCTANE options provide the means to fit OCTANE into a variety of existing computational settings. Add on PCI cards offer compatibility and inter-operability with other high performance networks. SCSI, Fibre Channel PCI and XIO adapters support additional storage devices, maintaining a high quality, high speed connection to the OCTANE system. Additionally, third-party software that supports connectivity to personal computers and Apple® Macintosh® systems, allows OCTANE to integrate well into existing heterogeneous working environments.

There are eight standard OCTANE configurations. Four OCTANE/SI standard models, three with single processors and one with dual CPUs. They have clock speeds of either 175MHz or 195MHz, 64MB or 128MB main memory, and 2GB or 4GB of internal disk space. 4MB of texture memory are optional on the OCTANE/SI. The OCTANE/SSI comes with either single or dual processors, a clock speed of 195MHz, 128MB or 256MB of memory and 4GB of disk space. The top of the line, OCTANE/MXI system, like the OCTANE/SSI, has either single or dual processors, a clock speed of 195MHz, 128MB or 256MB of memory and 4GB of disk space. In addition, hardware-accelerated texture is built-in to the OCTANE/MXI, including 4MB of dedicated texture memory. (See Table 7.1.) All configurations include a 20-inch monitor, audio microphone, stereo speakers, keyboard, and mouse.

Table 7.1 Standard OCTANE Configurations

| GFx | Texture | CPUs | Clock Speed | Memory | Disk | Free XIO slots | Marketing Code |
|---|---|---|---|---|---|---|---|
| /SI | Optional | 1 | 175MHz | 64MB | 2GB | 3 | WT5-1P175SI2 |
| /SI | Optional | 1 | 195MHz | 64MB | 2GB | 3 | WT5-1P195SI2 |
| /SI | Optional | 1 | 195MHz | 128MB | 4GB | 3 | WT5-1P195SI4 |
| /SI | Optional | 2 | 175MHz | 64MB | 2GB | 3 | WT5-2P175SI2 |
| /SSI | Optional | 1 | 195MHz | 128MB | 4GB | 2 | WT5-1P195SSI4 |
| /SSI | Optional | 2 | 195MHz | 128MB | 4GB | 2 | WT5-2P195SSI4 |
| /MXI | Included | 1 | 195MHz | 128MB | 4GB | 2 | WT5-1P195MXI4 |
| /MXI | Included | 2 | 195MHz | 128MB | 4GB | 2 | WT5-2P195MXI4 |
| All configurations include 20-inch monitor, audio microphone, stereo speakers, keyboard, and mouse | | | | | | | |

## 7.1 CPU

With an architecture optimized for the advanced features of the MIPS R10000 processor, the OCTANE compute engine can unleash the complete power of one or two R10000 processors to accelerate real world application software. The R10000 can deliver two to three times the performance of previous generations of processors. The symmetric multiprocessing (SMP) architecture gives users the choice of how to apply the power: two processors can be used to quickly solve one task or to simultaneously solve two previously separate problems, such as engineering design and analysis.

The unique crossbar architecture allows data to flow from point to point within the system at high speeds without interuption. The crossbar hardware supports a unique feature called priority I/O, detailed in Section 2.1, Architectural Overview. Priority I/O allows application software to allocate and manage the bandwidth available within the system. This unique bandwidth management scheme can guarantee that a critical data transfer, such as loading a 3D model from memory to the screen, receives the necessary bandwidth to remain interactive. OCTANE combines powerful CPU capabilities, advanced graphics, and a highly flexible and fast I/O subsystem with an innovative system architecture. The result is a low latency, high bandwidth system that is optimzed for premier application performance.

Single processor machines can easily be upgraded to dual processor machines at any time.

See Section 2.2, R10000 Processor for more information.

## 7.2 Memory and Storage

The standard OCTANE/SI configurations have either 64MB or 128MB of Memory and 2- or 4GB of internal disk space. The standard OCTANE/SSI and OCTANE/MXI have 128MB of Memory and 4GB of internal disk space. Additionally, SCSI, Fibre Channel PCI and XIO adapters can be added to support multiple RAID disk arrays and other mass storage devices for large or critical data stores.

The unique efficiency of the OCTANE system architecture and the Synchronous DRAM-based main memory subsystem make a 1GB per second main memory peak bandwidth possible. Two Ultra SCSI channels provide 40MB per second interfaces for optimized data transfers to and from internal or external hard disks, floppies, CD-ROMs, and/or tape drives.

OCTANE comes with JEDEC standard DIMMs that are available in various sizes. Memory is configured as four banks of two DIMMs each. Memory can only be installed in DIMM pairs -- referred to as banks. Memory from Silicon Graphics is available in DIMM banks. This results in memory upgrades of 64MB, 128MB and 256MB. Banks can receive any valid size (32MB, 64MB or 128MB) DIMM, making the current maximum capacity 1GB. A 512MB bank is planned that will double the memory potential to 2GB.

See Section 2.4, Memory System for more information.

## 7.3 Graphics Configurations

OCTANE delivers a high level of graphics performance to the desktop by making extensive use of dedicated processing hardware. OCTANE graphics, combined with the power of one or two R10000 compute engines, and OpenGL, the industry-standard open graphics library, provide optimal application performance.

The basic graphics acceleration subsystem for OCTANE includes one or two hardware Geometry Engine processors, dedicated rasterization, and the ability to take advantage of a texturing engine, if one is installed. The dedicated frame buffer memory is specifically tuned for handling 2D and 3D images and image processing operations. Advanced features include: alpha blending, accumulation buffering, anti-aliased RGB lines and points, texture mapping, fog, numerous lighting features, arbitrary clipping planes, depth cueing, soft shadow and depth of field, sub-pixel positioning, stenciling, stereo graphics, pan and zoom, and X11 pixel operations.

### 7.3.1 OCTANE/SI

OCTANE/SI, the entry-level graphics subsystem, is well suited for solid modeling applications. It brings high-end desktop graphics performance to mainstream engineers and technical users. The SI system includes a single Geometry Engine (GE11) processor, one Raster Engine (RE4), two Pixel Engines (PP1), and 12MB of frame buffer memory. The SI graphics option card fills only one XIO slot, leaving three free slots for high-speed networking and peripheral options.

The standard configuration ‘OCTANE/SI with texture’ comes with a Texture Engine (TE) for SI Graphics. The OCTANE/SI without texture can be reconfigured at any time with the additon

of the optional hardware accelerated texture subsystem. The addition of the texture subsystem does not use up any additional slots.

See Section 4.1.1, Solid Impact (SI) and Section 4.1.2, Solid Impact with Texture Option for more information.

### 7.3.2 OCTANE/SSI

The OCTANE/SSI graphics subsystem has two hardware Geometry Engine processors, two Raster Engines, four Pixel Engines, and 24MB of frame buffer memory for twice the solid modeling performance of an SI subsystem. An SSI graphics option card fills two XIO slots.

OCTANE/SSI is the ideal machine for large solid modeling projects, mechanical analysis, pre- and post-production processing, and untextured 3D animation. If requirements change, hardware texture support can be added at any time -- effectively upgrading the SSI to a top-of-the-line MXI subsystem.

See Section 4.1.3, Super Solid Impact (SSI) for more information.

### 7.3.3 OCTANE/MXI

The OCTANE/MXI graphics subsystem delivers the same, high performance graphics processing power as the SSI, with the addition of a built-in hardware accelerated texture subsystem that includes 4MB of dedicated texture memory and two Texture Engines. The MXI graphics option card requires two XIO slots.

OCTANE/MXI is the right choice for users with demanding visualization needs, such as simulation, digital prototyping, virtual reality, and extremely complex 3D models.

See Section 4.1.4, Maximum Impact Option (MXI) for more information.

### 7.3.4 Graphics Specifications:

- Geometry Engine$^{TM}$: 960MFLOPS
- RDRAM Frame Buffer: 32-bit double buffer with Z-stenciling; (whether or not this can be done simultaneously depends on the video output format and available frame buffer memory)
- Raster Engine: 120M pixel per second fill rate
- Texture Engine: zoom, warp, rotate images
- Texture Cache: 4MB - optional on OCTANE/SI and OCTANE/SSI systems

## 7.4 Upgrades

Thanks to its modular design, an OCTANE can be upgraded as a user's needs and situation change. For instance, the CPU is implemented as a daughtercard of the motherboard, making an upgrade from a single to dual processor system relatively simple. Memory, texture, geometry, and graphics can be upgraded as well. This scalability ensures that OCTANE can not only fill the evolving needs of the user, but also take advantage of future hardware

technologies and keep up with the increasing performance requirements of mainstream and leading-edge application software.

### 7.5 OCTANE Options

The OCTANE system architecture is highly flexible. By adding more memory, a second processor, more graphics power or internal disks, even an entry-level, single processor OCTANE/SI system can be expanded and scaled as required by changing needs. A number of graphics, storage, networking, video and other options are available for further customization and optimization of the system. Options include: Fibre Channel, four port Ultra SCSI, four port ATM OC3, Serial-HIPPI, four port 100Base-T Ethernet, OCTANE Digital Video, OCTANE Personal Video, OCTANE Compression, Presenter, a 24-inch monitor (for /SSI and /MXI systems only) and dual heads. All XIO option cards have the same form factor and cover one slot, with the exception of the OCTANE/SSI and OCATANE/MXI graphics cards that require two slots.

OCTANE products also support the Peripheral Component Interconnect expansion bus at 266MB per second, providing access to a wide range of network and I/O adapters. A PCI card cage allows OCTANE to combine leading performance and compatibility with the most popular industry standards.

Six of the seven ports of the OCTANE crossbar are used to support three categories of I/O devices: Baseline, PCI option cards and XIO option cards. One port is dedicated to baseline I/O activities, one port to PCI bus and four ports are open to support high-performance graphics, video, display, networking and peripheral option cards. The state-of-the-art built-in I/O provides up to 27GB of internal storage. The advanced XFS file system allows users to stripe across Ultra SCSI disks for very fast data processing or video I/O.

Baseline

- 10/100Base-TX autosensing full/half duplex Ethernet networking built-in for LANs with high grade category 5 wiring
- 1 internal and 1 external fast/wide single ended Ultra SCSI bus (40MB per second peak per bus)
- built-in Ultra SCSI is single-ended; differential Ultra SCSI is available on a PCI card or XIO MSCSI; a third party adapter can be used to convert single-ended to differential
- 3 x 3.5 inch SCA device drive bays
- 2GB, 4GB and 9GB Ultra SCSI drives
- 2 x 450K baud IBM AT standard serial ports -- additional serial ports can be added via PCI card
- 1 x parallel port IEEE 1284 standard  EPP/ECP compliant
- audio includes analog, AES serial digital, and ADAT optical digital

### 7.5.1 Storage XIO Option Cards:

#### 7.5.1.1 Fibre Channel -- two ports (one slot)

Fibre Channel is a high-speed multiport XIO™ networking device that will eventually accommodate TCP/IP as well. Fibre Channel PCI adapters will support multiple RAID disk arrays and other mass storage devices for large or critical data stores. The optics-based data transfer system insure a higher standard of data integrity than conventional wire-based systems can provide.

#### 7.5.1.2 Four Port Ultra SCSI (one slot)

The single card Ultra SCSI provides four additional channels, each at a 40MB per second transfer rate, for optimized data transfer to and from external hard disks, floppies, CD-ROMs, and tape drives. All four ports are differential only. The board is limited to 100MB of total throughput.

### 7.5.2 Networking XIO Option Cards:

#### 7.5.2.1 Four Port ATM OC3 (one slot)

The IRIS Multiport ATM OC3 network adapter is an excellent solution for applications that require constant or nearly constant data rates, such as video-on-demand or multiple, simultaneous streams with guaranteed bandwidth.

The IRIS Multiport ATM OC3 network adapter includes two onboard RISC processors and four independent Synchronous Optical Network (SONET) OC3 ports (155.52Mb per second). The XIO ATM network adapter can also provide full-duplex throughput on all ports simultaneously. The ports support multimode fiber-optic SC connectors.

The IRIS Multiport ATM OC3 network adapter is designed specifically for the new Scalable Shared-memory MultiProcessing ($S^2MP$™) and OCTANE architectures from Silicon Graphics. Depending on the applications, the network adapter can support up to 256 virtual channels (VCs) per port. It has 4MB of local memory per port shared between receive and transmit functions, and 512KB of local control memory per port for VC tables, cell scheduling tables, and received cell buffers.

The IRIS Multiport ATM OC3 network adapter also includes:

- a character device API for environments that require CBR traffic or other custom applications
- a VC management program (atmarp) for IP over PVC configurations
- an ILMI management daemon, with SNMP MIB accessible through either ATM ports or other IP networking interfaces

The IRIS Multiport ATM OC3 network adapter fully complies with industry standards, such as versions 3.0 and 3.1 of the ATM Forum's ATM User-Network Interface standard. It supports ATM adaptation layer 5 (AAL5) over Constant Bit Rate (CBR), and best-effort traffic (UBR), and all standard IP applications (through SVCs and/or PVCs), using best-effort traffic contracts in compliance with RFC 1577 (Classical IP over ATM).

#### 7.5.2.2 Serial-HIPPI -- one port (one slot)

Serial-HIPPI is an excellent gigabit technology for moving large volumes of data. Silicon Graphics is the leading provider of HIPPI connectivity solutions.

IRIS® Serial-HIPPI, a single-port network interface that conforms to the ANSI High-Performance Parallel Interface-Serial (Serial-HIPPI) Specification, Revision 2.3, implements short-wavelength, fiber-optic-based Serial-HIPPI to provide 800Mb per second in each direction simultaneously. IRIS Serial-HIPPI leads the industry with TTCP rates exceeding 720Mb per second using TCP/IP over a HIPPI network.

The IRIS Serial-HIPPI network adapter is a single slot (half-size) XIO™ board. All communication with the host is DMA-based using the scatter/gather model. Multiple descriptor rings drastically reduce system interrupts.

The IRIS Serial-HIPPI network adapter features:

- four MIPS® RISC processors
- 8.5MB of onboard memory
- onboard IP checksum calculation
- Independent hardware support for each direction
- capability to generate up to 128 READY credits
- self-testing loopback mode

HIPPI-Bypass, a proprietary, low-latency, high-bandwidth protocol, enables very low-latency communication between hosts. The protocol bypasses the conventional network processing overhead, allowing any user-level process to send and directly receive messages to and from the network adapter while preserving page-based protection mechanisms.

#### 7.5.2.3 4 port 100Base-T Ethernet (one slot)

One 100Base-T port comes standard with all of the new generation systems. Silicon Graphics 100Base-T products support the TX interface and can autosense 100Base-T or 10Base-T for backward compatibility with existing networks.

100Base-T is the most popular low-cost solution for increased desktop bandwidth. Because 100Base-T and Ethernet use the same CSMA/CD method, packet size, and format, 100Base-T can easily be integrated into existing networks. The ease of upgrading existing networks to 100Base-T makes it the most attractive technology when existing networks become saturated or new stations are added.

For expansion with optimal performance, the optional four-port 100Base-T XIO network adapter is tuned for high-performance multiprocessing systems and features:

- onboard local memory with store-and-forward architecture minimizing overhead and packet delivery latency
- interrupt batching techniques minimizing interrupts, PIOs per packet, and CPU load

- buffer and descriptor formats designed to minimize copying, and IP checksumming performed in the hardware, reducing the need for the operating system and driver to touch data

### 7.5.3 Video XIO Option Cards:

#### 7.5.3.1 OCTANE Digital Video (one slot)

OCTANE Digital Video provides the same industry-leading performance as the Indigo2 IMPACT™ Video board, with additional features such as video texturing for unique special effects.

OCTANE Digital Video features include:

- similar features to IMPACT Video
- 2 x 10-bit CCIR-601 video I/O streams - that can be linked together as video and key
- a real-time path to and from the graphics screen or to and from main memory
- a video to TRAM interface with auto mip-map generation
- a high quality color space converter
- support for 24-bit packed RGB to conserve disk space

Silicon Graphics is the platform for uncompressed video processing. It supports uncompressed non-linear editors to complement the strong paint, compositing and graphics software packages that are available. Increased pixel transfer rates of OCTANE graphics make paint and compositing applications fly.

The OCTANE Digital Video board provides two input and two output channels of SMPTE 259M, CCIR-601 serial digital video. The video can be PAL or NTSC timing and 8- or 10-bits per component. The two 4:2:2 inputs can be used together for a dual-link signal with video and key. The supported signal formats are in Table 6.2. All formats support embedded error detection and handling (EDH) to ensure pristine signal quality.

Both streams can be routed directly to and from main memory or the graphics screen in real time. The memory interface of the Digital Video board can be programmed for a variety of formats, including packed 24-bit RGB to save on disk space. In some formats, video can be streamed in real time to disk using the built-in external Ultra SCSI (40MB per second) interface or an optional Fibre Channel interface card. Using an industry standard third party A/D or D/A converter allows the digital video to be converted to a range of different analog signal formats.

The OCTANE Digital Video board has a built-in high-quality color space converter that uses a 24-bit internal data path and 15-bit coefficients to ensure accuracy and diminish the signal degradation often associated with color conversion in the past. This allows RGB images generated within the computer to be converted to the YUV color space of traditional video equipment with minimal distortion. The converter also incorporates a patent-pending constant hue hardware unit to maintain the highest quality even for extreme YUV colors when converting from YUV to RGB. The color space converter provides a peak error rate of .1 percent for one pass and 4.2 percent for 100 round trip conversions, giving users the highest-quality imagery without degradation.

The OCTANE Digital Video board also has a built-in real-time interface to the graphics texture system. This interface allows a single stream of full frame-rate video with an alpha or key channel, or two streams of field-rate video to be texture mapped onto 3D geometry with real-time mipmapping for high image quality. These real-time video textures can be used to create true three-dimensional digital video effects. Since the texture-mapped polygons can be manipulated in real time using the OCTANE graphics hardware, users can create an unlimited number of innovative new effects such as shattering glass or grains of sand. Video texturing can also be used by three-dimensional animation applications to add high levels of detail to a scene by means of live display panels or video billboards.

Table 7.2 OCTANE Digital Video Signal Formats

| Format | Resolution | Number of Inputs | Number of Outputs | Timing |
|---|---|---|---|---|
| 4 : 2 : 2 | 8- or 10-bits | 2 | 2 | PAL/NTSC |
| 4 : 4 : 4 | 8- or 10-bits | 1 | 1 | PAL/NTSC |
| 4 : 2 : 2 | 8- or 10-bits | 1 | 1 | PAL/NTSC |
| 4 : 4 : 4 | 8- or 10-bits | 1 | 1 | PAL/NTSC |
| RP-175 | 8- or 10-bits | 1 | 1 | PAL/NTSC (RGB) |

#### 7.5.3.2 OCTANE Personal Video (one slot)

Personal Video is a low-cost video processing card that is compatible with all OCTANE systems. It allows users to create and manipulate content for a variety of uses including: collaboration, video conferencing, multimedia presentations and multimedia Web sites.

OCTANE Personal Video offers many of the features of the OCTANE Digital Video board, but at a lower price. The Personal Video board provides both composite and digital video I/O ports, plus the reference timing input required for professional work. The digital video I/O port accepts the input of the (bundled) O2™ digital camera, and it becomes an industry-standard 8-bit CCIR-601 video I/O port when an external adapter (available from a third party) is added. OCTANE Personal Video uses the same high-quality color space converter found in the Digital Video board. The Personal Video board can capture the entire 1280x1024 graphics screen or just a portion of it, scales it down to video resolution, and streams it to video out and to main memory. Main memory may also be chosen as the source for real time video output. The analog composite video output signal quality is suitable for broadcast and easily times into a plant.

Personal Video enables video conferences for professional users, who demand a very good output signal quality. The O2 cam port can be converted to serial digital CCIR-601 using an adapter available from Miranda Inc.

Screen captures -- an important ability in the CAD world -- are facilitated by OCTANE Personal Video. Three-dimensional movies of a model can be captured, scaled down, compressed (using software compression), and stored to disk. Digital media tools can then be used to add a title, or piece together several different sequences. The resulting movie can be

dropped into the out-box of a web server or played to a VCR. OCTANE Personal Video supports this powerful new way to communicate.

OCTANE Personal Video features include:

- an affordable, analog video board for collaboration
- a high quality analog signal sufficient for many broadcasters
- a high quality color space converter
- the collaboration features of O2 -- screen capture and video conferencing among others
- the new digital media tools bundled with IRIX 6.4
- bundled O2 cam and InPerson software

The OCTANE Personal Video board takes full advantage of the digital media tools bundled with every OCTANE system. The bundled tools provide the means for developing compelling digital media content for design reviews, presentations, and Web pages that incorporate video, as well as audio and 3D graphics. Tools are available for capturing, editing, and converting audio, video, and images of various file formats. For example, MediaRecorder is a capture tool for audio, video, screen, and camera data and MediaPlayer can be used for fast, convenient viewing of many types of time-based media.

OCTANE Personal Video can turn any application into a video source by allowing any portion of the screen to be recorded directly to disk. By using screen capture capabilities, an engineer can demonstrate a design concept by creating a compressed video image of a model interaction and storing the image to disk. The video image can be edited using the bundled intuitive media editing tools, and then either published to a Web page using the OutBox personal Web server or output to video tape.

MediaPlayer supports Silicon Graphics and QuickTime™ movies and can be used as a stand-alone player or with other media tools. Captured movies can be edited using MovieMaker, a user friendly tool for editing multitrack movie files. MovieMaker includes filters for adding special A/V effects and a title palette for adding graphics and text to movies. SoundTrack supports MovieMaker by allowing editing of multiple independent audio tracks. Additionally, bundled software, such as ImageWorks, can be used to edit single frames.

#### 7.5.3.3 OCTANE Compression (one slot)

Bundled software utilities (MediaConvert and dmplay) allow users to take rendered frames, convert them to YUV, compress them to disk, then play them back as full frame rate video. This is a valuable asset for 3D animators and analysis engineers who want to motion test a rendered sequence and see the result on an interlaced, YUV video monitor. High quality compression capabilities are also required for broadcast weather graphics applications.

- OCTANE Compression:
  - based on IMPACT Compression
  - 2 streams of Motion JPEG at ratios as low as 2:1 for high image quality
  - on board analog I/O for preview or broadcast playback of compressed video
  - direct connection to OCTANE Digital Video for 2 streams of I/O

OCTANE Compression provides high-quality compression capabilities that can be used for anything from Web-based movie-making to high-end broadcast graphics. The OCTANE Compression board provides two streams of motion JPEG compression with ratios as low as 2:1. This state-of-the-art compression engine can compress video as it is captured, or video that is resident in memory (for example rendered frames). The compression engine has a hardware scaler and color space converter in the loop to handle input YUV or RGB video of different sizes. The compression card has a direct connection to the OCTANE Digital Video I/O card, so two streams of 601 video can be independently compressed or decompressed in real time. The OCTANE Compression card has a composite and S-Video input and output port, as well as an analog genlock loop-through.

The flexible architecture of the OCTANE Compression board allows an OCTANE workstation to replace a traditional digital disk recorder for many applications such as 3D animation. It allows artists to render a test sequence and then play it back as full-resolution video displayed on an interlaced PAL or NTSC monitor. Using the bundled conversion software utility, rendered frames can be hardware compressed and stored to disk. The sequence can then be decompressed and played back at full resolution for display on an external monitor or on the graphics screen.

#### 7.5.3.4 Video Option Specifications

Table 7.3 OCTANE Video Products Specifications

| Parameter | Digital Video | Personal Video | Compression |
|---|---|---|---|
| Input format | 2x10 bit CCIR-601 | 1x Analog,<br>1x O2 cam | 1x Analog |
| Input connector | 75 ohm BNC terminated, unbalanced | 75 ohm BNC terminated, unbalanced | 75 ohm BNC terminated, unbalanced |
| **Input Characteristics:** | | | |
| Return loss | 15dB@270MHz | | |
| Output format | 2x10 bit CCIR-601<br>75 ohm BNC terminated | 1 x Analog,<br>1 x SGI digital<br>75 ohm BNC terminated | 1 x Analog<br>75 ohm BNC terminated |
| **Output Characteristics:** | | | |
| Freq. Response | N/A | 4.5MHz (-0.5 dBa) | 4.2MHz (-0.5dBa) |
| | | 5.5MHz (-3 dBa) | 5.5MHz (-3 dBa) |
| Color weighted S/N | N/A | 48 dBa | 48 dBa |
| Differential phase | N/A | < 2.5% | < 2.5% |
| Differential gain | N/A | < 2 degrees | < 2 degrees |
| Amplitude | 800mv +/-10% | N/A | N/A |
| Rise and fall time | .4ns to 1. 5ns | N/A | N/A |
| Overshoot | <10% peak to peak | N/A | N/A |
| Clock jitter | <740ps p/p<br>10Hz-10KHz | N/A | N/A |
| **Feature Summary** | | | |
| Graphics capture | X | X | |
| Color space conversion | X | X | X |
| Video texture | X | | |
| Scaling | | X | X |
| M-JPEG | | | X |
| Blender | X | | |

Table 7.3 OCTANE Video Products Specifications (Continued)

| Parameter | Digital Video | Personal Video | Compression |
|---|---|---|---|
| $O^2$ cam support | | X | |
| Input format | 2x10 bit CCIR-601 | 1x Analog,<br>1x O2 cam,<br>CCIR 601 via dongle | 1x Analog |

### 7.5.4 Audio Option Card

Every OCTANE workstation comes with an extensive suite of built-in audio capabilities including:

- Microphone
- Stereo desktop loudspeakers with headphone output
- Stereo analog line level I/I
- Stereo digital coaxial and optical I/O
- 8-channel ADAT Optical digital I/O

In addition, each PCI audio option card offers:

- 8-channel 24-bit ADAT Optical I/O
- Stereo 24-bit AES3-1992 I/O (coaxial and optical); this also serves as AES11 synchronization I/O
- Professional jitter attenuation on digital audio input clocks
- Video Composite Sync Loop-Through: This PAL/NTSC synchronization source professionally locks audio sample rates to video
- Sample-accurate synchronization with other digital media subsystems

### 7.5.5 Other OCTANE Options

#### 7.5.5.1 Presenter

A 13-inch diagonal flat panel display, the 1280 Presenter features 1280x1024 pixel resolution, 18-bit true color and 24-bit color with frame rate modulation, sleep mode switch, and camera mount support. Also supported is a 12-inch diagonal flat panel display with 1024x768 pixel resolution, 12-bit true color, and 15-bit color with dithering between pixels. Both 1024 and 1280 Presenter have a digital display interface, custom backlight inverter, and presentation-quality audio. Presenter products are portable and perfect for walk-through design reviews with customers, team collaboration, and other interactive presentations.

#### 7.5.5.2 Dual Heads

For applications that require additional screen space, the desktop family supports a dual-head option. For programming flexibility, dual-head configurations support independent windows

on each head for advanced data modeling and analysis applications. For example, one head can display a high-level view of the application data while the other head remains available for interactive analysis of the data. The dual head option also supports multiple screen views for simulation and training purposes.

#### 7.5.5.3 High-Resolution 24-inch Monitor

Available as an upgrade to the standard 20-inch monitor for OCTANE/SSI and OCTANE/MXI workstations only, the 24-inch monitor supports the display of virtually any output resolution or pixel timing. The high-resolution 24-inch monitor handles requirements ranging from VGA to 1600x1200, including 1600x1000 at 72Hz, to take advantage of the wide aspect ratio of the display. It is also capable of displaying up to 1920x1080 at 60Hz for high density television purposes.

#### 7.5.5.4 Single Port OCTANE Channel Option (OCO)

The OCTANE Channel Option is a multi-channel alternative that splits the frame buffer for output to 1, 2 or 4 monitors at various resolutions. It is primarily useful for applications requiring wrap around simulation or head mounted, three-dimensional displays.

Table 7.4 OCO Output Formats

| Resolution | Timing | Number of Channels |
|---|---|---|
| 640 x 486 interlaced | component NTSC/RS-170 (RGB) | 4 |
| 640 x 480 non-interlaced | VGA<br>Field sequential<br>VGA (Full scene anti-aliasing) | 4<br>2<br>1 |
| 800 x 486 interlaced | RS170-Field sequential<br>RS170-Field parallel component | 2<br>2 |
| 800 x 600 non-interlaced | SVGA | 2 |
| 875 x 808 interlaced | Field sequential | 2 |
| 1025 x 946 interlaced | Field sequential | 2 |